Wuxi Unigroup Microelectronics CO.,LTD.

60V N-Channel Trench MOSFET(Preliminary)

General Description

- Trench Power technology
- Low $R_{DS(ON)}$) 2 Ω
- Low Gate Charge
- Low Input and Output Leakage
- 2000 V ESD Protection

Applications

- Synchronous Rectification in DC/DC and AC/DC Converters
- Isolated DC/DC Converters in Telecom and Industrial

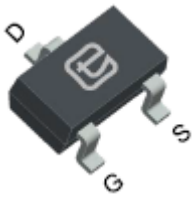
Product Summary

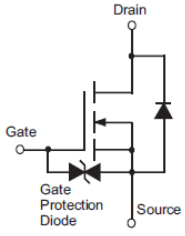
V_{DS}	60V
I_D (at V_{GS}=10V)	0.35A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 2Ω

100% UIS Tested

RoHS

SOT-23





Part Number	Package Type	Form	Marking
TTX2N7002KA	SOT-23	Tape&Reel	7002KA

Absolute Maximum Ratings (T_A =25ºC unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current B	T_C =25ºC	I_D	300	mA
	T_C =100ºC		190	
Pulsed Drain Current A		I_{DM}	800	mA
Power Dissipation C	T_C =25ºC	P_D	0.35	W
	T_C =100ºC		0.14	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	ºC

Thermal Characteristics

Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient	Steady-State	$R_{\Theta JA}$	300	ºC/W

Electrical Characteristics(T_J =25ºC unless otherwise noted)							
Symbol	**Parameter**	**Conditions**		**Value**			**Units**
				Min	**Typ**	**Max**	
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D =10uA,V_{GS} =0V		60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =60V, V_{GS} =0V	T_J =25ºC	--	--	1	μA
			T_J =100ºC	--	--	500	
I_{GSS}	Gate-Body Leakage Current	V_{DS} =0V, V_{GS} =±20V		--	--	±10	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA		1	--	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} =10V, I_D =0.35A		--	--	2	Ω
		V_{GS} =4.5V, I_D =0.35A		--	--	4	Ω
g_{FS}	Forward Transconductance	V_{DS} =10V, I_D =0.35A		100	--	--	ms
V_{SD}	Diode Forward Voltage	I_S =0.2A, V_{GS} =0V		--	--	1.3	mV
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS} =0V, V_{DS} =25V, f =1MH_Z		--	40	--	pF
C_{oss}	Output Capacitance			--	18	--	
C_{rss}	Reverse Transfer Capacitance			--	3.6	--	
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS} =4.5V,V_{DS} =10V, I_D =0.25mA		--	0.8	--	nC
Q_{gs}	Gate Source Charge			--	0.45	--	
Q_{gd}	Gate Drain Charge			--	0.2	--	
$T_{D(on)}$	Turn-On Delay Time	V_{DD} = 30 V, R_L = 150 Ω I_D = 200 mA, V_{GEN} = 10 V, R_G = 10 Ω		--	28	--	ns
$T_{D(off)}$	Turn-Off Delay Time			--	40	--	

A. Single pulse width limited by maximum junction temperature.

B. The maximum current rating is package limited.

C. The power dissipation P_D is based on $T_{J(MAX)}$ =175ºC, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

Typical Characteristics T_J = 25ºC, unless otherwise noted

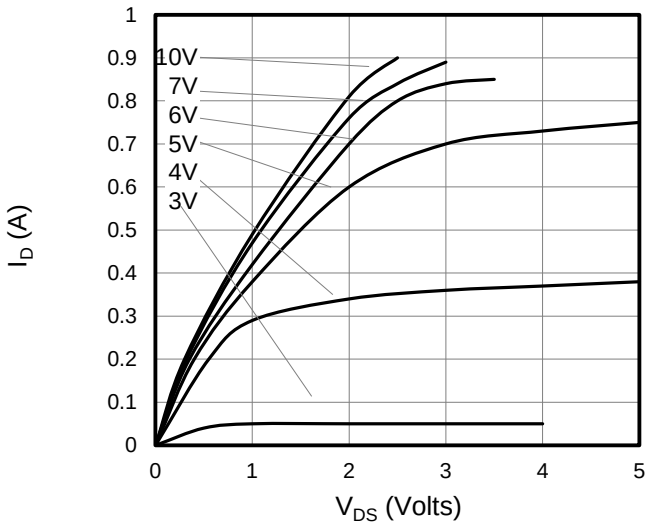


Figure 1: On-Region Characteristics

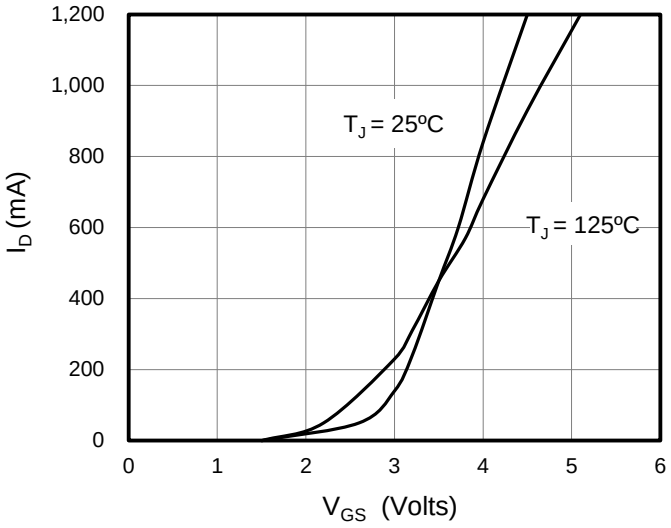


Figure 2: Transfer Characteristics

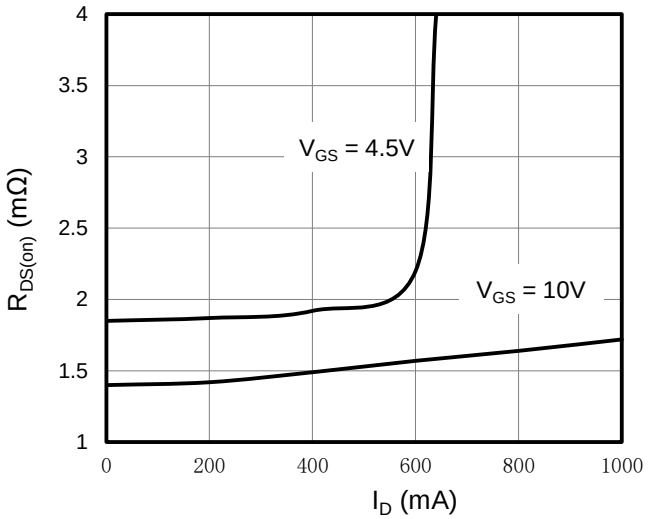


Figure 3: On-Resistance vs. Drain Current

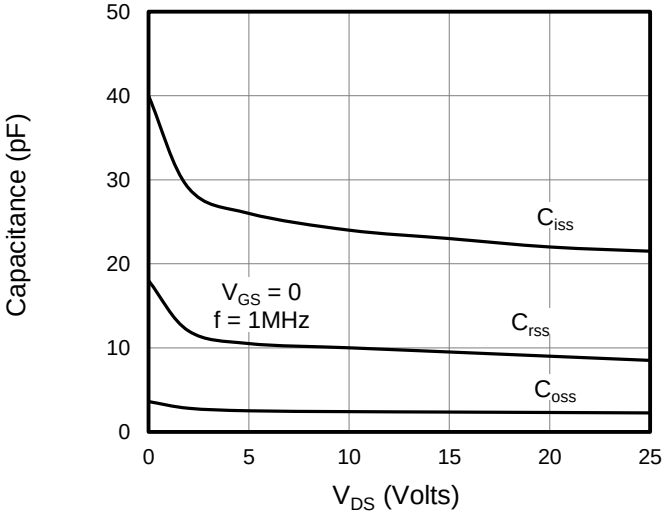


Figure 4: Capacitance Characteristics

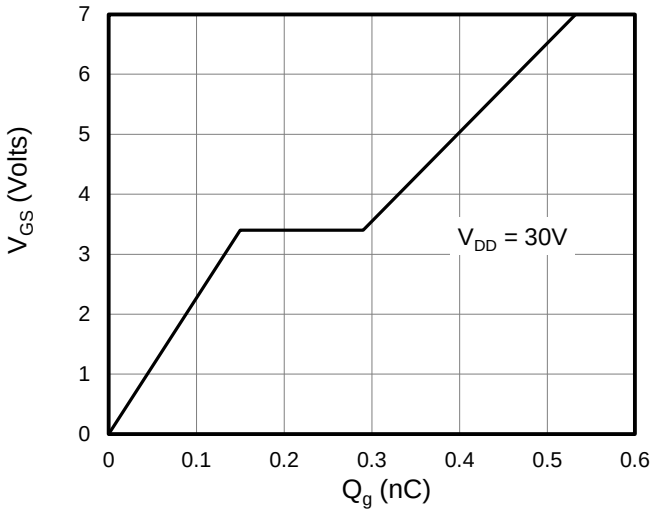


Figure 5: Gate Charge Characteristics

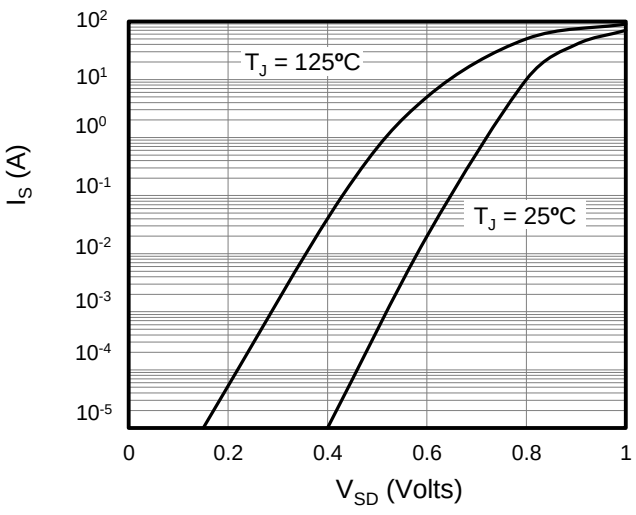


Figure 6: Body Diode Forward Voltage

Typical Characteristics T_J = 25ºC, unless otherwise noted

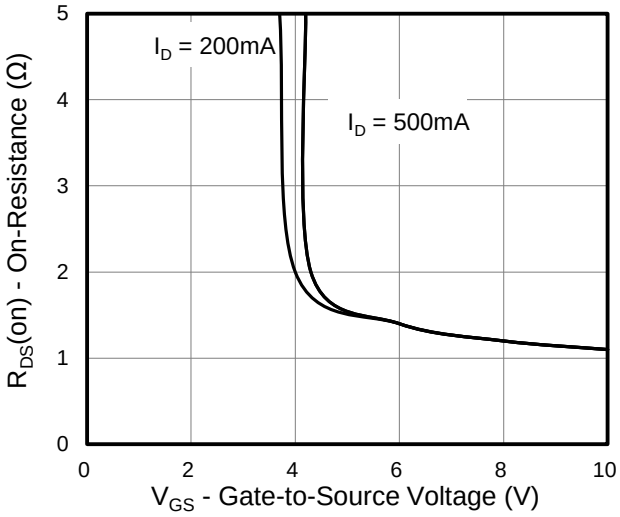


Figure 7: On-Resistance vs. Junction Temperature

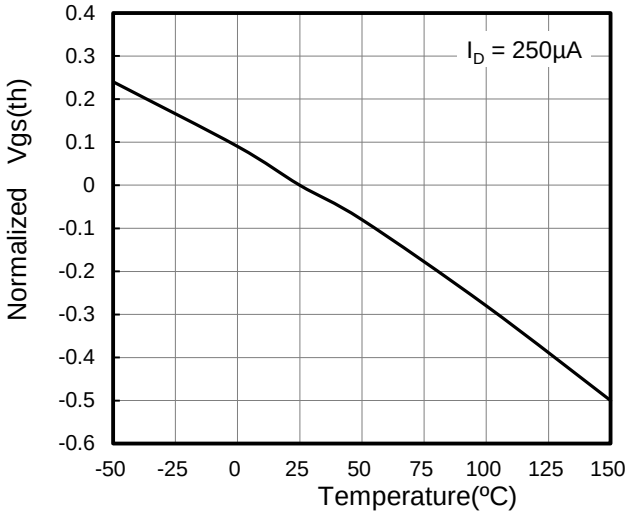


Figure 8: Vgs(th) vs. Junction Temperature

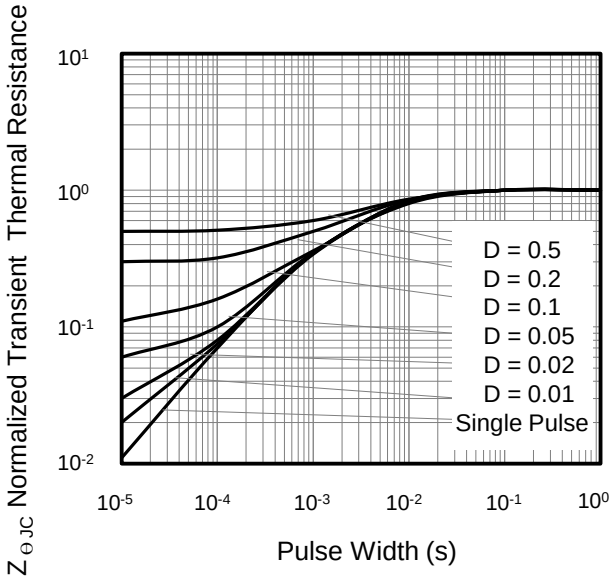


Figure 9: Normalized Transient Thermal Resistance

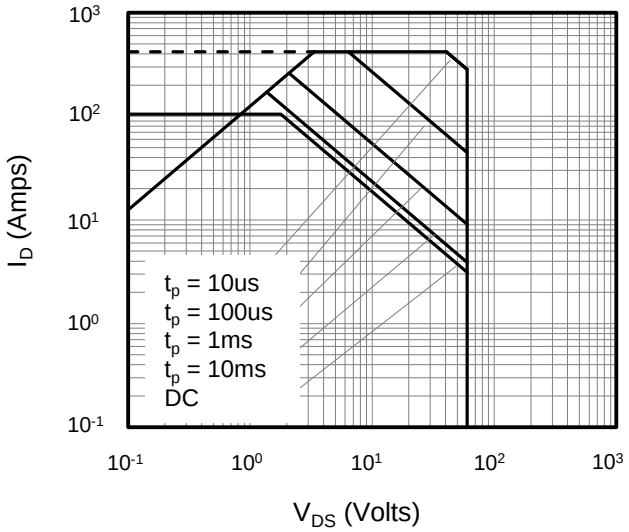


Figure 10: Safe Operating Area

Figure A：Gate Charge Test Circuit and Waveform

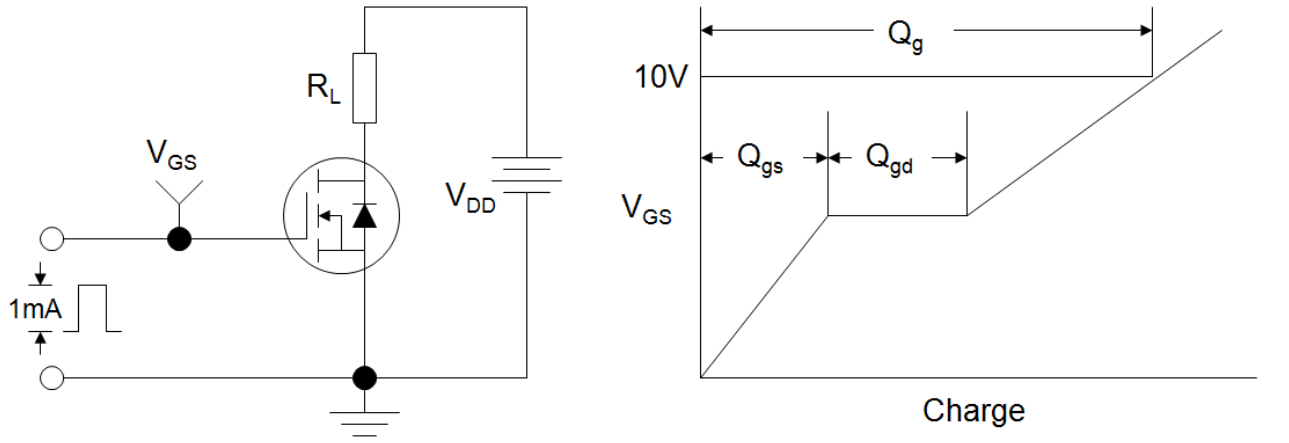


Figure B：Resistive Switching Test Circuit and Waveform

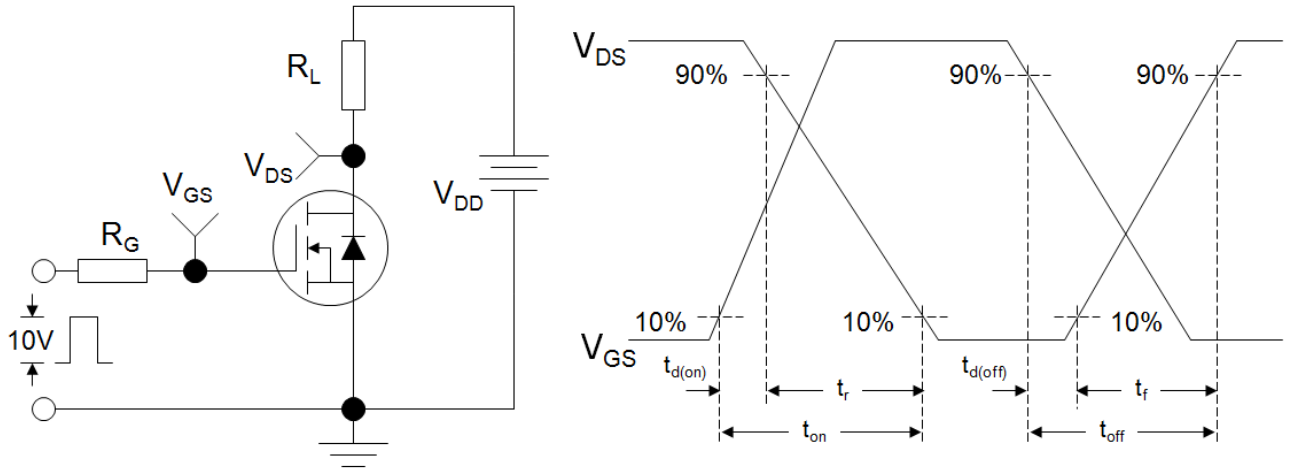
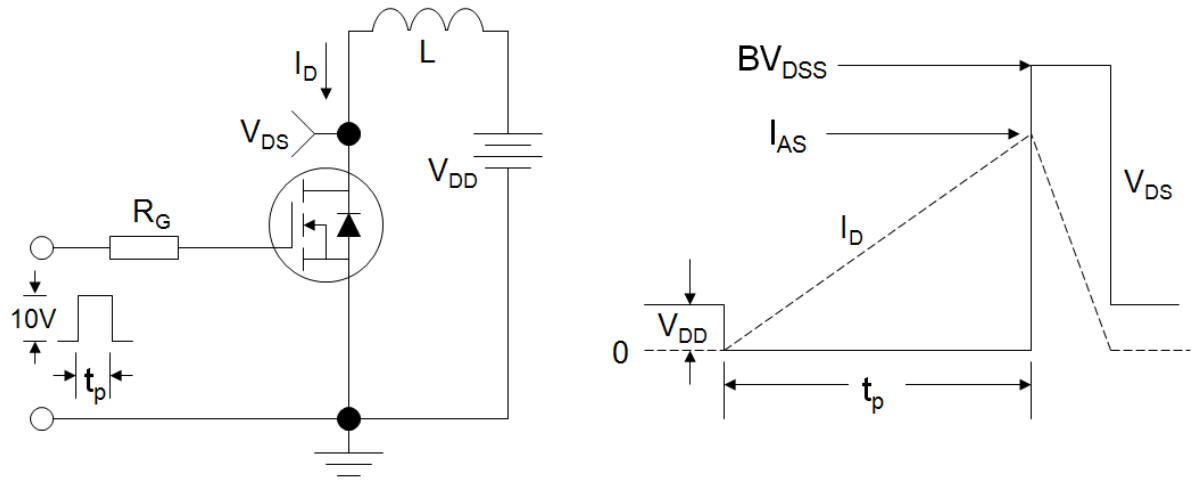
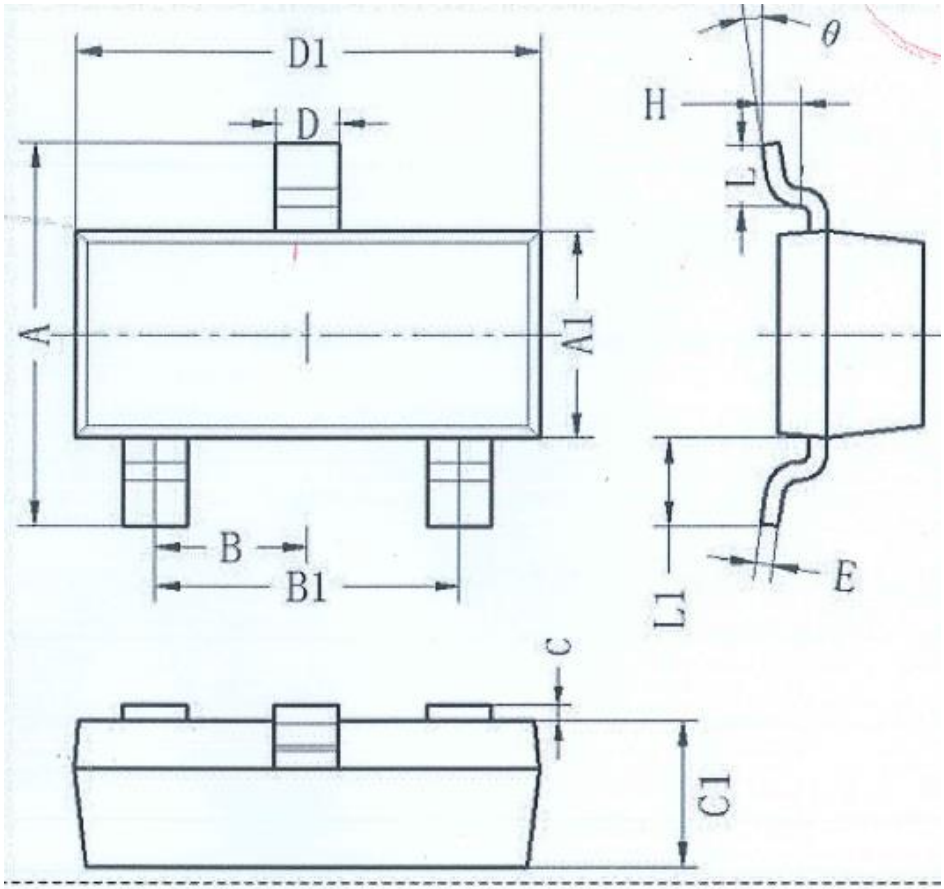


Figure C：Unclamped Inductive Switching Test Circuit and Waveform



SOT-23(封装厂 N)



符号	标准	下公差	上公差	下限值	上限值
A	2.4	-0.15	0.15	2.25	2.55
A1	1.3	-0.1	0.1	1.2	1.4
B	0.95	-0.05	0.05	0.90	1.00
B1	1.9	-0.1	0.1	1.8	2
C	0.08	-0.06	0.06	0.02	0.14
C1	0.95	-0.05	0.05	0.9	1
D	0.4	-0.1	0.1	0.3	0.5
D1	2.9	-0.1	0.1	2.8	3
E	0.1	-0.03	0.03	0.07	0.13
H	0.25	-0.03	0.03	0.22	0.28
L	0.4	-0.1	0.1	0.3	0.5
L1	0.55	-0.07	0.07	0.48	0.62
θ	4	-3	3		7

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