

30V N-Channel Trench MOSFET(Preliminary)

General Description

- Trench Power Technology
- Low R_{DS(ON)}
- Low Gate Charge
- Optimized for fast-switching Applications

Applications

- Synchronous Rectification in DC/DC and AC/DC Converters
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

VDS 30V

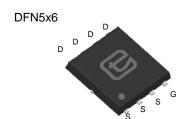
 I_D (at V_{GS} =10V) 120A

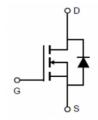
 $R_{DS(ON)}$ (at V_{GS} =10V) < 3.4m Ω

 $R_{DS(ON)}$ (at V_{GS} =4.5V) < 4.7m Ω

100% UIS Tested







Device Package		Form	Marking
TTG120N03AT	DFN5x6	Tape&Reel	120N03AT

Absolute Maximum Ratings $T_C = 25^{\circ}C$, unless otherwise noted						
Parameter		Symbol	Value	Unit		
Drain-Source Voltage		V _{DS}	30	V		
Gate-Source Voltage		V _{GS}	±20	V		
Continuous Drain Current B	T _C = 25°C		51	А		
Continuous Drain Current B	$T_{\rm C} = 100^{\rm o}{\rm C}$	I _D	51			
Pulsed Drain Current ^A		I _{DM}	360	Α		
Avalanche Current A		I _{AS}	30	Α		
Single Pulse Avalanche Energy L =0.3mH ^A		E _{AS}	135	mJ		
Dower Dissipation C	T _C = 25°C	P _D	127	W		
Power Dissipation ^C	$T_{\rm C} = 100^{\rm o}{\rm C}$	P _D	82	W		
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 175	°C		

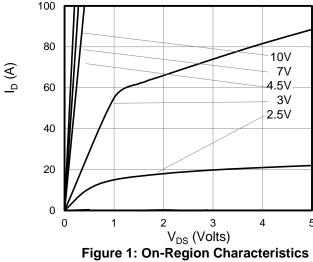
Thermal Resistance					
Parameter		Symbol	Value	Unit	
Thermal Resistance, Junction-to-Case	Steady-State	$R_{\Theta JC}$	1.24	°C/W	
Thermal Resistance, Junction-to-Ambient	Steady-State	$R_{\Theta JA}$	100		



Electric	cal Characteristics(T _J =25°C ur	nless otherwise r	oted)				
Complete Day	Deremeter	Conditions		Value			11!1
Symbol	Parameter			Min	Тур	Max	Units
STATIC P	ARAMETERS					_	
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250µA,V _{GS} =0V		30	-		V
I _{DSS} Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V	T _J =25°C			1		
	Zelo Gale Vollage Dialii Guiterii	$V_{DS} = 30V, V_{GS} = 0V$	T _J =100°C			25	μA
I _{GSS}	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$			-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		1	1.7	2.4	V
<u> </u>	Statio Dunin Course On Registeres	V _{GS} =10V, I _D =20A			2.6	3.4	mΩ
R _{DS(ON)} Static Drain-Source	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{V}, I_D = 20 \text{A}$		3.6	4.7	mΩ	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =20A		24.16			S
V_{SD}	Diode Forward Voltage	I _S =30A, V _{GS} =0V				1	V
Is	Maximum Body-Diode Continuous Current B					51	Α
DYNAMIC	PARAMETERS					•	
C _{iss}	Input Capacitance				2113		
C _{oss}	Output Capacitance	$V_{GS} = 0V, V_{DS} = 15V, f = 1MH_Z$			801		pF
C _{rss}	Reverse Transfer Capacitance				356		
SWITCHIN	NG PARAMETERS						
Q_g	Total Gate Charge				89		
Q_{gs}	Gate Source Charge	$V_{GS} = 10V, V_{DS} = 15V, I_{D} = 50A$			9		nC
Q_{gd}	Gate Drain Charge				16		
t _{D(on)}	Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 15V, I_{D} = 50A,$ $R_{G} = 3\Omega$			12		
t _r	Turn-On Rise Time				11		ns
$T_{D(off)}$	Turn-Off Delay Time				40		
t _f	Turn-Off Fall Time				12		
t _{rr}	Body Diode Reverse Recovery Time				60		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =30A, di/dt =100A/μs			120		nC

- A. Single pulse width limited by maximum junction temperature.
- B. The maximum current rating is package limited.
- C. The power dissipation P_D is based on $T_{J(MAX)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

Typical Characteristics $T_J = 25^{\circ}\text{C}$, unless otherwise noted



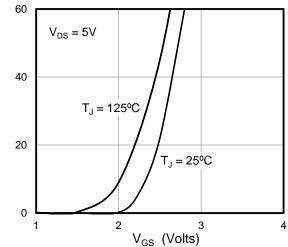


Figure 2: Transfer Characteristics

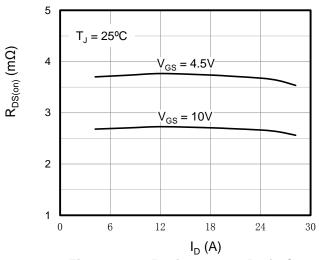


Figure 3: On-Resistance vs. Drain Current

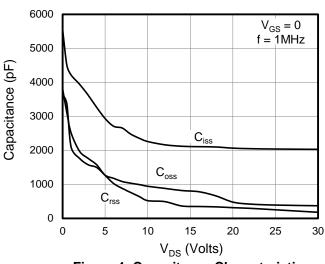


Figure 4: Capacitance Characteristics

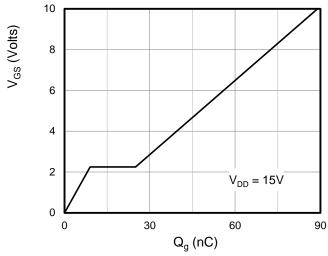


Figure 5: Gate Charge Characteristics

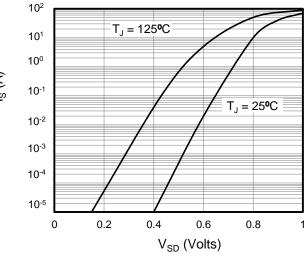
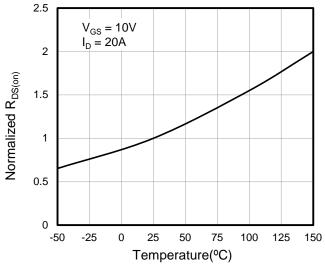


Figure 6: Body Diode Forward Voltage

Typical Characteristics $T_J = 25^{\circ}\text{C}$, unless otherwise noted



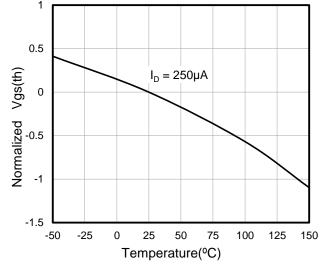
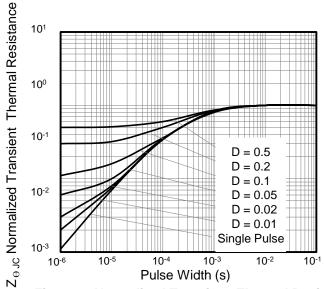


Figure 7: On-Resistance vs. Junction Temperature

Figure 8: Vgs(th) vs. Junction Temperature



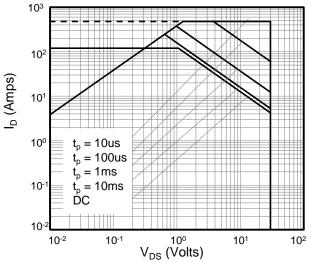


Figure 9: Normalized Transient Thermal Resistance

Figure 10: Safe Operating Area



Figure A: Gate Charge Test Circuit and Waveform

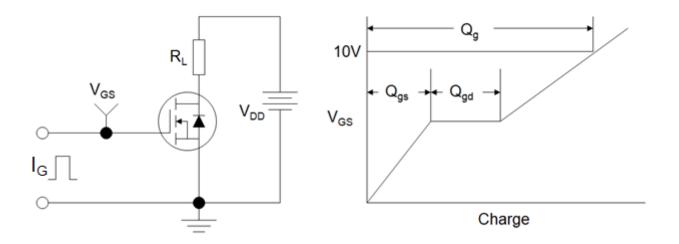


Figure B: Resistive Switching Test Circuit and Waveform

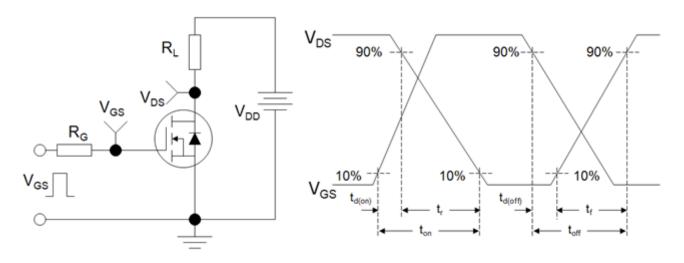
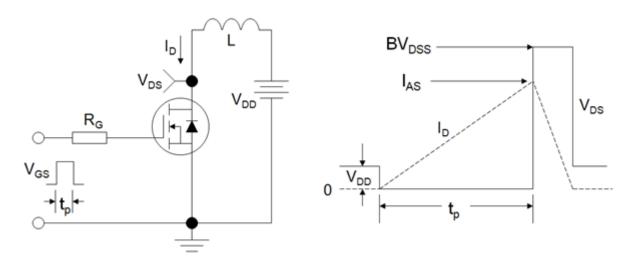
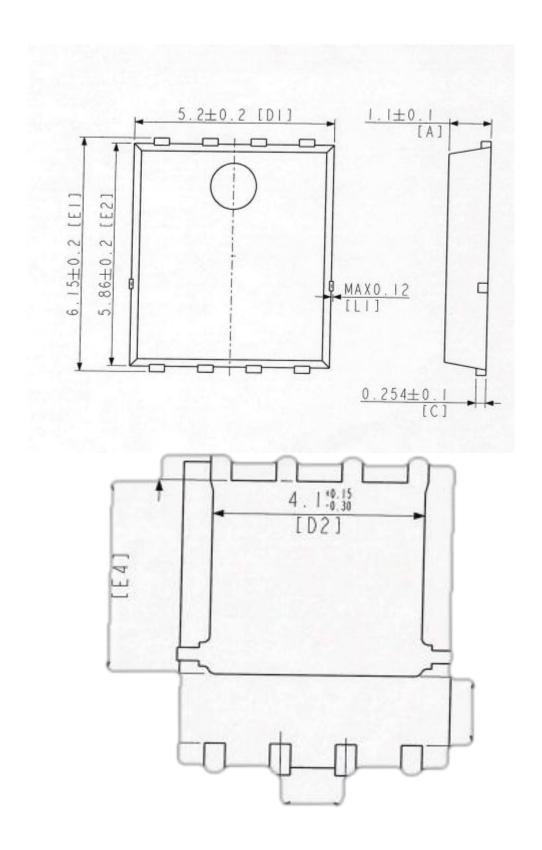


Figure C: Unclamped Inductive Switching Test Circuit and Waveform





DFN5x6(H)





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