





80V N-Channel DTMOS

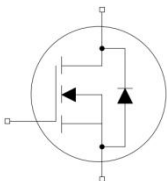
<p>General Description</p> <ul style="list-style-type: none"> ● Trench Power SGT technology ● Very low on-resistance $R_{DS(ON)}$ ● Low Gate Charge ● Excellent Gate Charge x $R_{DS(ON)}$ Product <p>Applications</p> <ul style="list-style-type: none"> ● High Frequency Switching and Synchronous Rectification 	<p>Product Summary</p> <p>V_{DS} 80V</p> <p>ID (at $V_{GS}=10V$) 155A</p> <p>$R_{DS(ON)}$ (at $V_{GS}=10V$) < 4.0mΩ</p> <p>100% UIS Tested</p> 
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TO-220



G D S

Drain



Gate

Source

Device	Package	Form	Marking
TSP15N08A	TO-220	Tube	P15N08A

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	155	A
	$T_C = 100^\circ C$		93	
Pulsed Drain Current ^A		I_{DM}	620	A
Avalanche Current ^A		I_{AS}	28	A
Single Pulse Avalanche Energy $L = 0.3mH$ ^A		E_{AS}	609	mJ
Power Dissipation ^C	$T_C = 25^\circ C$	P_D	208	W
	$T_C = 100^\circ C$		125	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ C$

Thermal Resistance				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Case	Steady-State	R_{thJC}	0.6	$^\circ C/W$
Maximum Junction-to-Ambient	Steady-State	R_{thJA}	60	



Electrical Characteristics($T_J = 25^\circ\text{C}$ unless otherwise noted)							
Symbol	Parameter	Conditions	Value			Units	
			Min	Typ	Max		
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	80	--	--	V	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	$T_J = 25^\circ\text{C}$	--	--	1	μA
			$T_J = 100^\circ\text{C}$	--	--	100	
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	--		± 100	nA	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	3	4	V	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{V}, I_D = 50\text{A}$	--	3.2	4.0	$\text{m}\Omega$	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 50\text{A}$	--	140	--	S	
V_{SD}	Diode Forward Voltage	$I_S = 50\text{A}, V_{GS} = 0\text{V}$	--	--	1	V	
I_S	Maximum Body-Diode Continuous Current ^B		--	--	50	A	
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$	--	7980	--	pF	
C_{oss}	Output Capacitance		--	562	--		
C_{rss}	Reverse Transfer Capacitance		--	98	--		
SWITCHING PARAMETERS							
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 40\text{V}, I_D = 50\text{A}$	--	129	--	nC	
Q_{gs}	Gate Source Charge		--	37	--		
Q_{gd}	Gate Drain Charge		--	31.4	--		
$t_{D(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 40\text{V}, I_D = 50\text{A}, R_G = 3\Omega$	--	54	--	ns	
t_r	Turn-On Rise Time		--	42	--		
$T_{D(off)}$	Turn-Off Delay Time		--	95	--		
t_f	Turn-Off Fall Time		--	19	--		
t_{rr}	Body Diode Reverse Recovery Time	$I_F = 30\text{A}, di/dt = 100\text{A}/\mu\text{s}$	--	52	--	ns	
Q_{rr}	Body Diode Reverse Recovery Charge		--	98	--	nC	

A. Single pulse width limited by maximum junction temperature.

B. The maximum current rating is package limited.

C. The power dissipation P_D is based on $T_{J(MAX)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

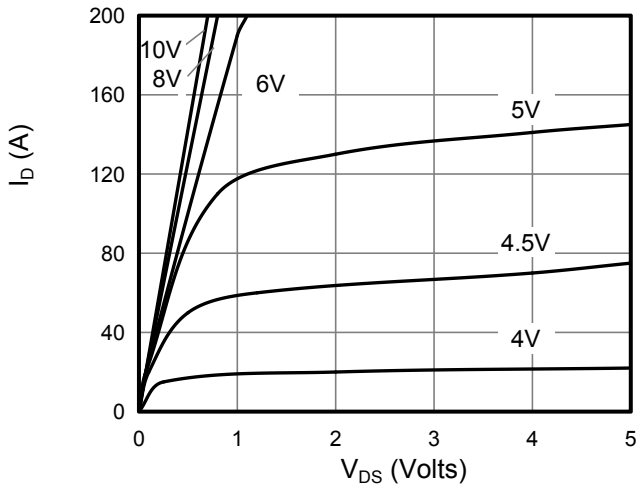


Figure 1: On-Region Characteristics

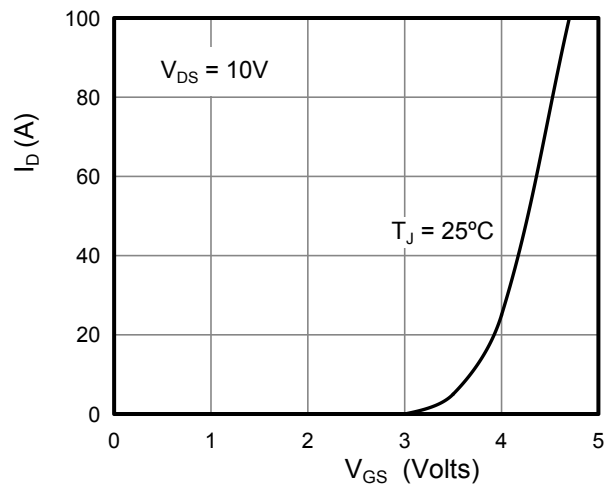


Figure 2: Transfer Characteristics

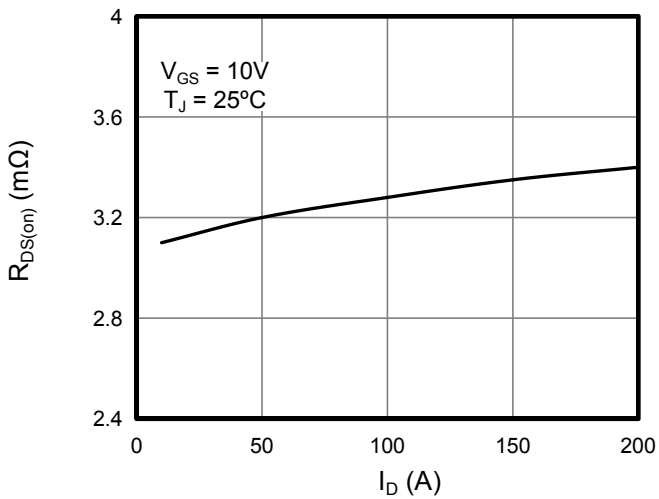


Figure 3: On-Resistance vs. Drain Current

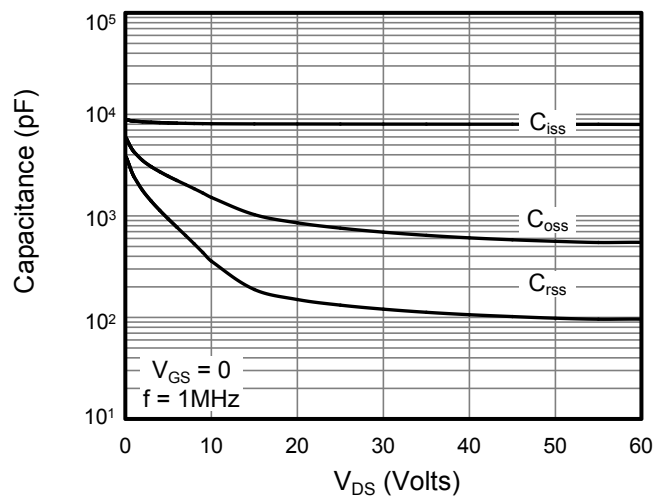


Figure 4: Capacitance Characteristics

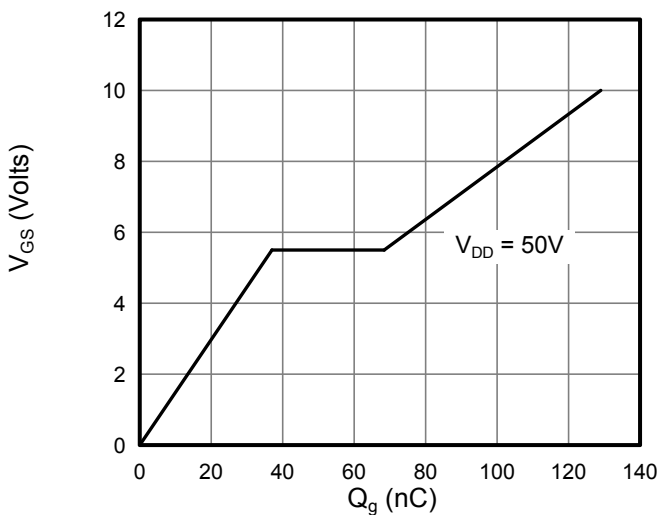


Figure 5: Gate Charge Characteristics

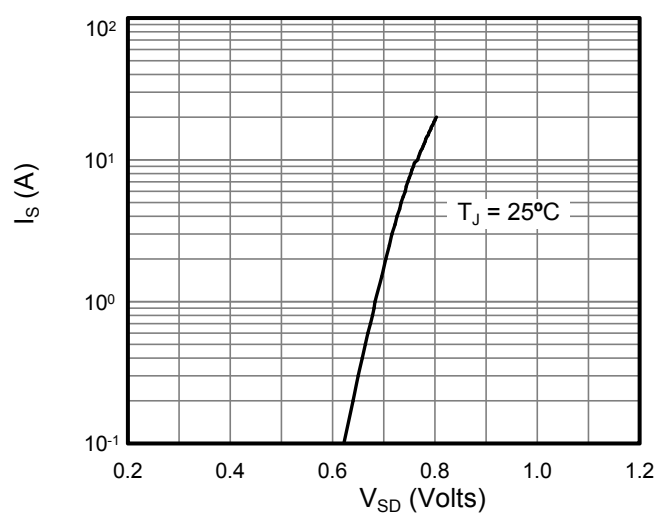


Figure 6: Body Diode Forward Voltage



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

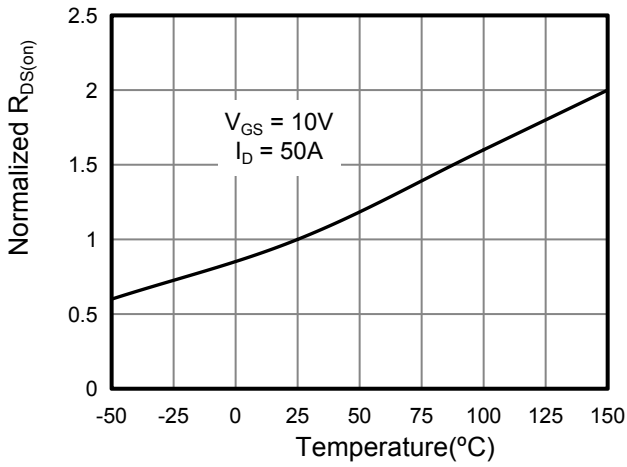


Figure 7: On-Resistance vs. Junction Temperature

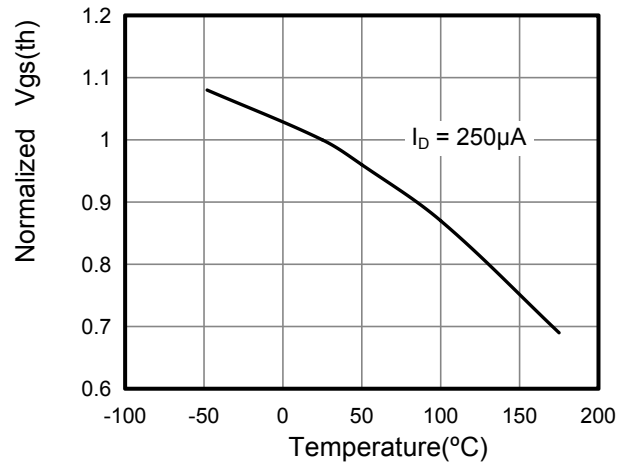


Figure 8: $V_{GS(th)}$ vs. Junction Temperature

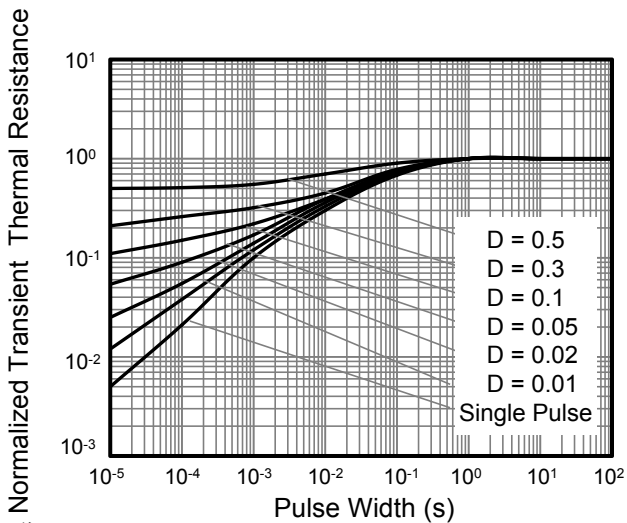


Figure 9: Normalized Transient Thermal Resistance

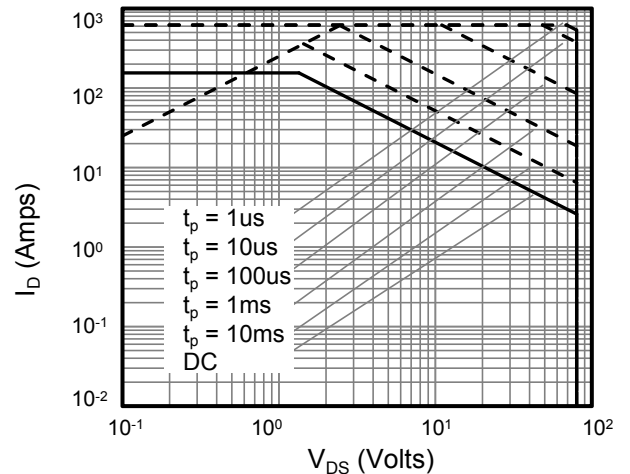


Figure 10: Safe Operating Area



Figure A: Gate Charge Test Circuit and Waveform

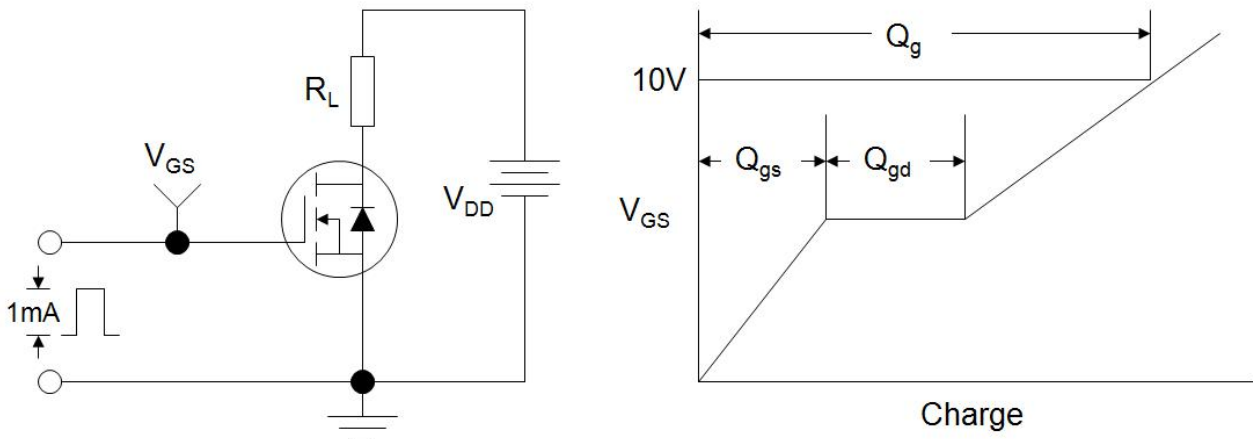


Figure B: Resistive Switching Test Circuit and Waveform

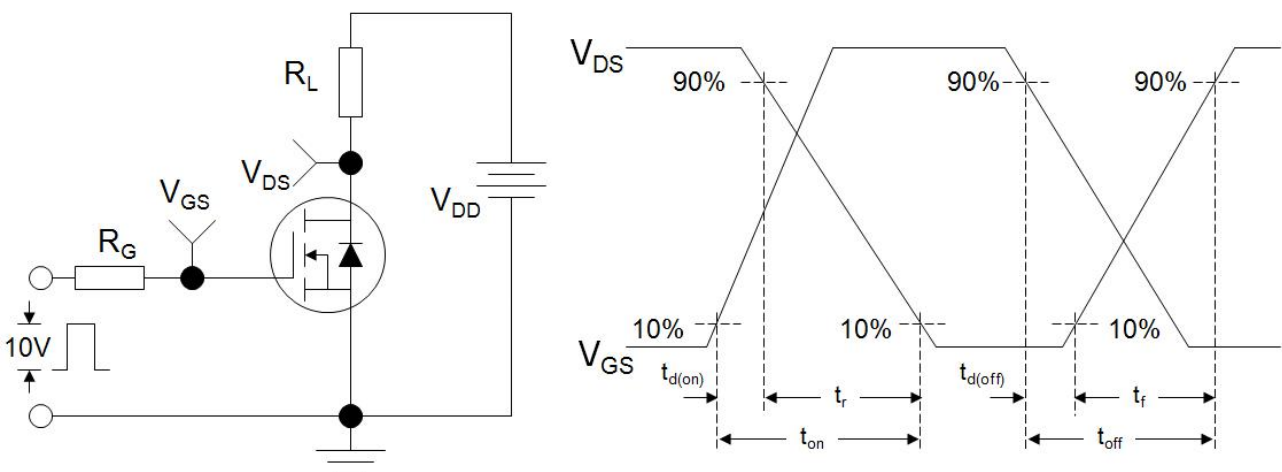
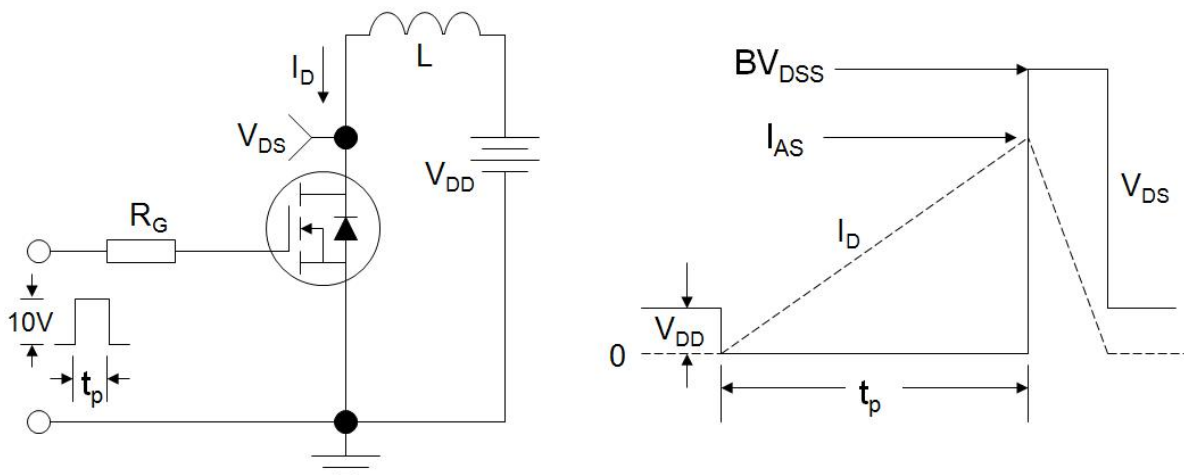
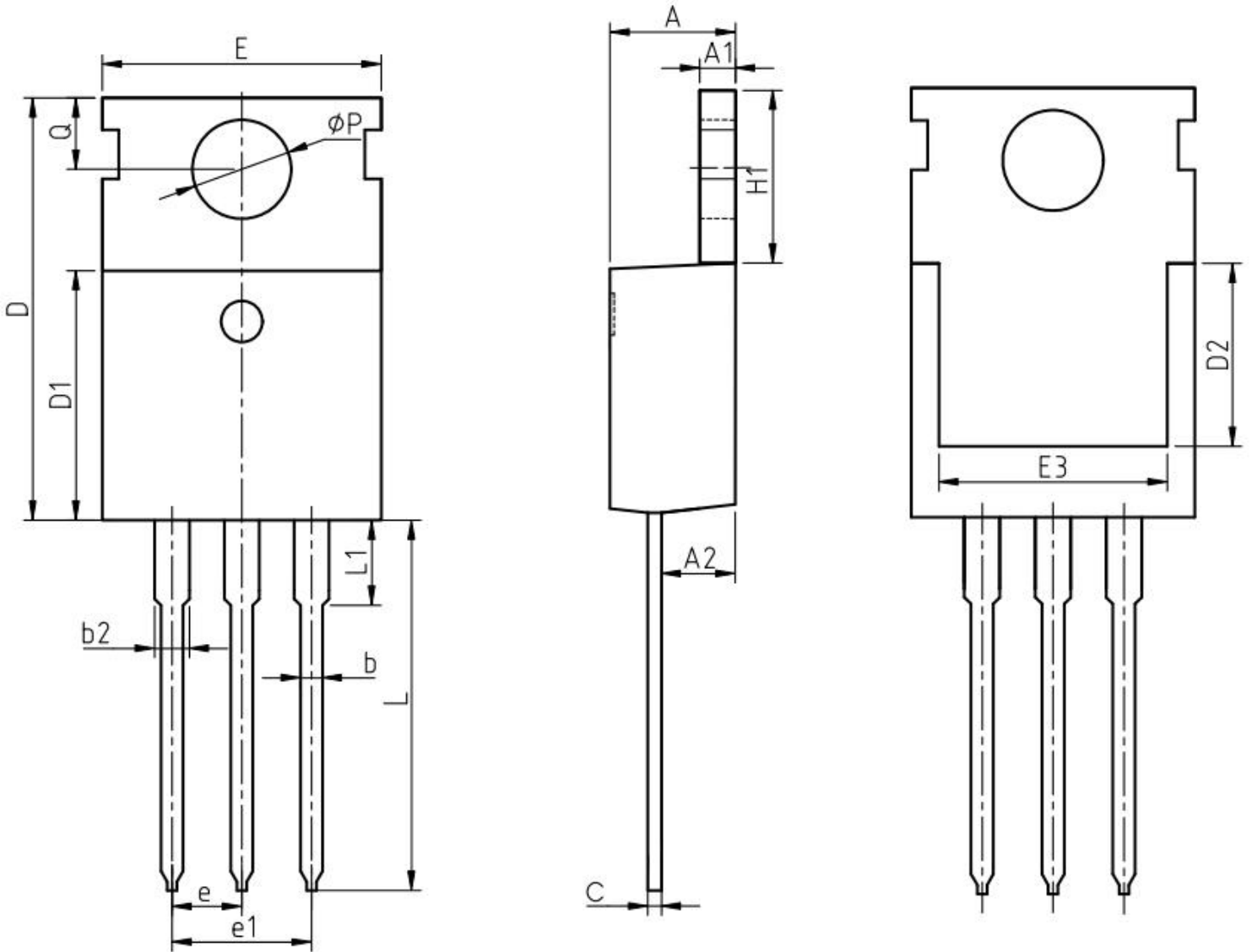


Figure C: Unclamped Inductive Switching Test Circuit and Waveform





TO-220 (封装厂 H)



Unit:mm			
Symbol	Min.	Nom	Max.
A	4.37	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.45	0.50	0.60
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-

Unit:mm			
Symbol	Min.	Nom	Max.
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ϕP	3.40	3.60	3.80
Q	2.60	2.80	3.00



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