

60V N-Channel Trench MOSFET

General Description

- Trench Power SGT technology
- Very low on-resistance R_{DS(ON)}
- Low Gate Charge
- Excellent Gate Charge x R_{DS(ON)} Product

Applications

• High Frequency Switching and Synchronous Rectification

Product Summary

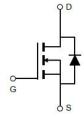
 V_{DS} 60V I_D (at $V_{GS} = 10V$) 60A $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 9mΩ $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 13.5mΩ

100% UIS Tested









Part Number	Package Type	Form	Marking	
TSG12N06AT	DFN5×6	Tape & Reel	D12N06AT	

Absolute Maximum Ratings (T_A =25°C unless otherwise noted)

			•		
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V_{GS}	±20	V	
Continuous Drain Current B	T _C =25°C	I _D	60	Δ.	
	T _C =100°C		36	Α	
Pulsed Drain Current A		I _{DM}	240	Α	
Avalanche Current A		I _{AS}	36	Α	
Single Pulse Avalanche Energy	L =0.3mH A	E _{AS}	65	mJ	
Power Dissipation ^C	T _C =25°C	P _D	56.5	W	
	T _C =100°C		44	W	
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 175	°C	
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Thermal Characteristics

Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Case	Steady-State	$R_{\Theta JC}$	1.7	0000		
Maximum Junction-to-Ambient	Steady-State	$R_{\Theta JA}$	50	°C/W		



Electrica	al Characteristics(T _J =25°C un	less otherwise r	oted)				
Cumbal	Devenueter	Conditions			Value		Units
Symbol	Parameter			Min	Тур	Max	
STATIC PA	RAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		60			V
	Zoro Cata Voltago Drain Current	nt $V_{DS} = 60V, V_{GS} = 0V$	T _J =25°C	-		1	μА
I _{DSS}	Zero Gate Voltage Drain Current		T _J =125°C	-		100	
I _{GSS}	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$		1		±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		1.1		2.5	V
ID.	Statia Drain Sauras On Basistanas	V _{GS} =10V, I _D = 20A			6.5	9	mΩ
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5V, I_D = 20A$			10.7	13.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A			85		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V				1	V
I _S	Maximum Body-Diode Continuous Current B					46	Α
DYNAMIC	PARAMETERS					•	
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f =1MH _Z			2455		pF
C _{oss}	Output Capacitance				240		
C _{rss}	Reverse Transfer Capacitance				34		
SWITCHIN	G PARAMETERS	•				•	
Q _g (10V)	Total Oaks Observe				45		
Q _g (4.5V)	Total Gate Charge	101/11 201/1	/// -30// I -20A		24		nC
Q_{gs}	Gate Source Charge	$V_{GS} = 10V, V_{DS} = 30V, I_{D} = 20A$			6.8		
Q_{gd}	Gate Drain Charge				11.5		
t _{D(on)}	Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 30V, I_{D} = 20A,$ $R_{G} = 3\Omega$			8		- ns
t _r	Turn-On Rise Time				3		
$T_{D(off)}$	Turn-Off Delay Time				25		
t _f	Turn-Off Fall Time				4		
t _{rr}	Body Diode Reverse Recovery Time	1 004 4:/// 5004/			25		ns
Q _{rr}	Body Diode Reverse Recovery Charge	-I _F =20A, di/dt =500A/μs			110		nC

- A. Single pulse width limited by maximum junction temperature.
- B. The maximum current rating is package limited.
- C. The power dissipation P_D is based on $T_{J(MAX)}$ =175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.



Typical Characteristics $T_J = 25^{\circ}\text{C}$, unless otherwise noted

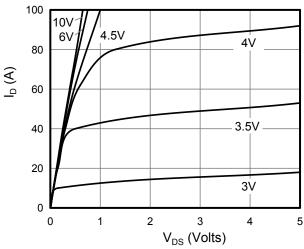


Figure 1: On-Region Characteristics **Characteristics**

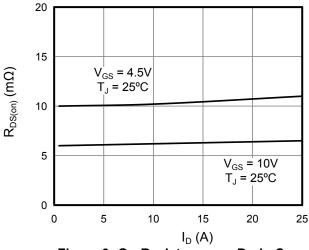


Figure 3: On-Resistance vs. Drain Current

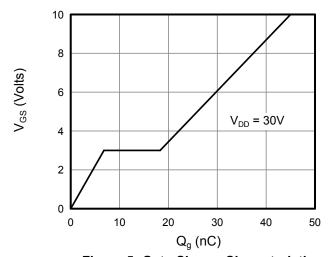
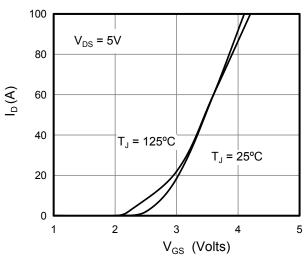


Figure 5: Gate Charge Characteristics



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Figure 2: Transfer

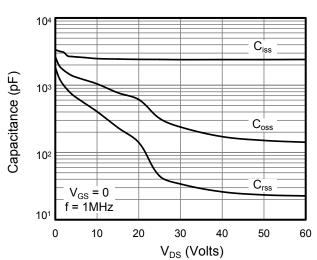


Figure 4: Capacitance Characteristics

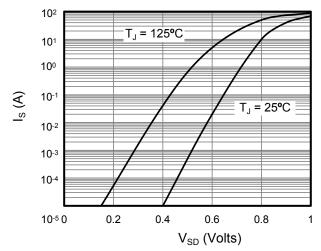
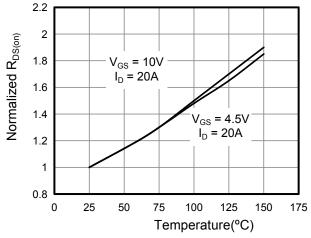


Figure 6: Body Diode Forward Voltage

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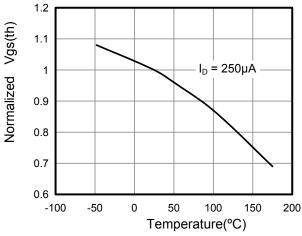
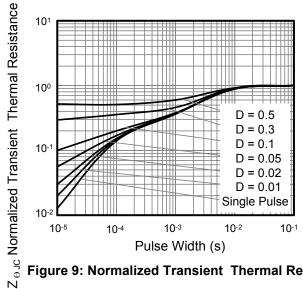


Figure 7: On-Resistance vs. Junction Temperature

Figure 8: Vgs(th) vs. Junction Temperature



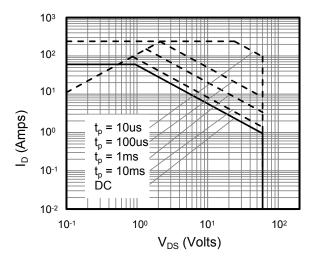


Figure 9: Normalized Transient Thermal Resistance

Figure 10: Safe Operating Area



Figure A: Gate Charge Test Circuit and Waveform

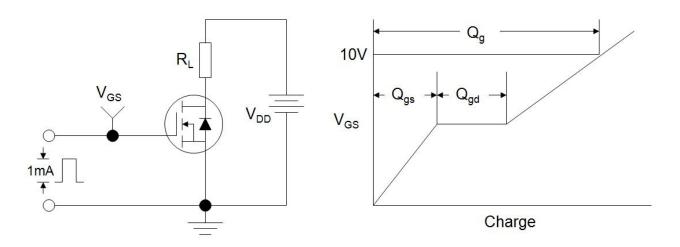


Figure B: Resistive Switching Test Circuit and Waveform

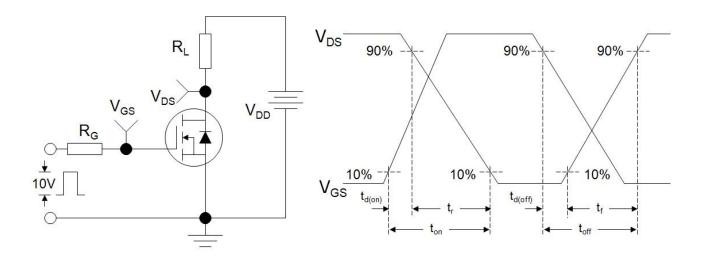
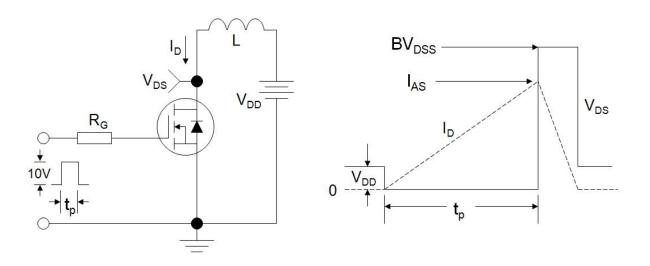
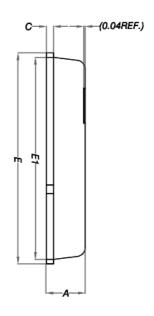


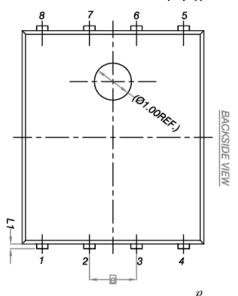
Figure C: Unclamped Inductive Switching Test Circuit and Waveform

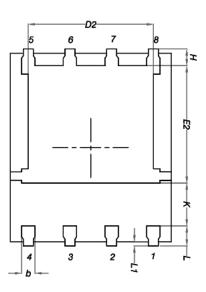


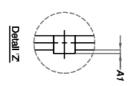


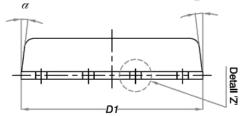
DFN5x6(封装厂M)











DIM.	MILLIMETERS			
	MIN.	NOM.	MAX.	
Α	0.90	1.00	1.10	
A1	0	-	0.05	
b	0.33	0.41	0.51	
С	0.20	0.25	0.30	
D1	4.80	4.90	5.00	
D2	3.61	3.81	3.96	
Ε	5.90	6.00	6.10	
E1	5.70	5.75	5.80	
E2	3.38	8 3.58 3.		
е	1.27 BSC			
Н	0.41	0.51	0.61	
K	1.10	-	-	
L	0.51	0.61	0.71	
L1	0.06	0.13	0.20	
α	0°	-	12°	



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