



650V Super-Junction Power MOSFET

DESCRIPTION

650V super-junction Power MOSFET

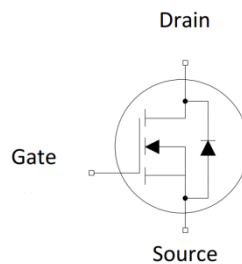
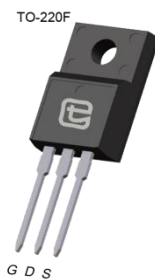
Super-junction power MOSFET is a revolutionary technology for high voltage power MOSFETs, designed according to the SJ principle. The SJ MOSFET is a price-performance optimized product enabling to target cost sensitive applications in Consumer and Lighting markets, designed by Wuxi Unigroup Microelectronics Company.

FEATURES

- Very low FOM $R_{DS(on)} \times Q_g$
- 100% avalanche tested
- RoHS compliant

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



Device Marking and Package Information

Device	Package	Marking
TPA65R180CFD	TO-220F	65R180CFD

Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.18	Ω
I_D	20	A
$Q_{g,typ}$	42	nC
I_{DM}	60	A



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted			
Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	650	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	20
		$T_C = 100^\circ\text{C}$	12
Pulsed Drain Current (note1)	I_{DM}	60	A
Gate-Source Voltage	V_{GSS}	± 30	V
Single Pulse Avalanche Energy (note2)	E_{AS}	500	mJ
Avalanche Current	I_{AS}	10	A
Power Dissipation	P_D	34	W
Continuous Body Diode Current	I_S	20	A
Pulsed Diode Forward Current (note1)	I_{SM}	60	
MOSFET dv/dt ruggedness, $V_{DS} = 0 \dots 400\text{V}$	dv/dt	50	V/ns
Reverse diode dv/dt, $V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$	dv/dt	50	V/us
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	$^\circ\text{C}$

Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	3.7	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	R_{thJA}	80	



Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	5	μA
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	--	--	5000	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5	--	4.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 10A$	--	0.155	0.18	Ω
Forward Transconductance (Note3)	g_{fs}	$V_{DS} = 10V, I_D = 10A$	--	14.5	--	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 50V,$ $f = 1.0\text{MHz}$	--	2484	--	μF
Output Capacitance	C_{oss}		--	114	--	
Reverse Transfer Capacitance	C_{rss}		--	1.23	--	
Total Gate Charge	Q_g	$V_{DD} = 520V, I_D = 20A,$ $V_{GS} = 10V$	--	42	--	nC
Gate-Source Charge	Q_{gs}		--	17	--	
Gate-Drain Charge	Q_{gd}		--	13	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 20A,$ $R_G = 25\Omega$	--	41	--	ns
Turn-on Rise Time	t_r		--	11	--	
Turn-off Delay Time	$t_{d(off)}$		--	103	--	
Turn-off Fall Time	t_f		--	7	--	
Drain-Source Body Diode Characteristics						
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 10A, V_{GS} = 0V$	--	0.86	1.2	V
Reverse Recovery Time	t_{rr}	$V_R = 520V, I_F = I_S,$ $di_F/dt = 100A/\mu s$	--	176	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.2	--	μC
Peak Reverse Recovery Current	I_{rrm}		--	14	--	A

Notes

1. Repetitive Rating: Pulse Width limited by maximum junction temperature
2. $V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse Width $\leq 300\mu s, \text{Duty Cycle } \leq 1\%$

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

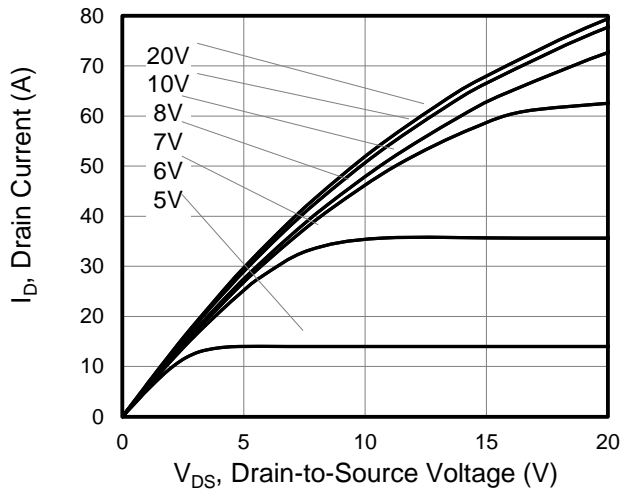


Figure 2. Transfer Characteristics

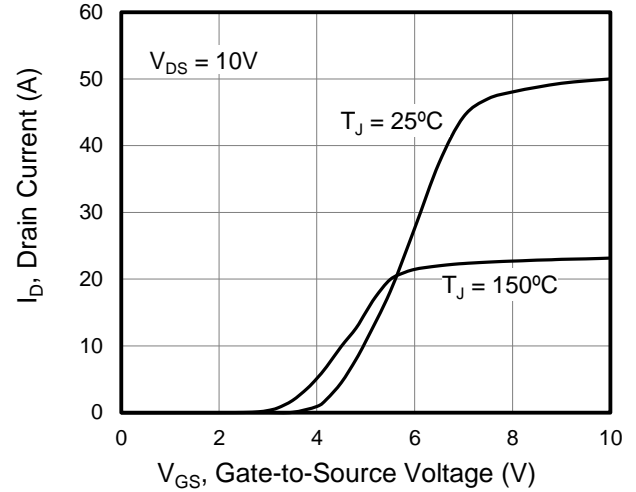


Figure 3. On-Resistance vs. Drain Current

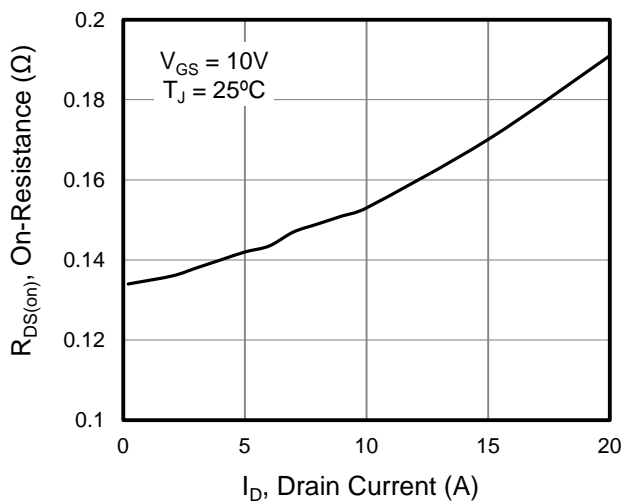


Figure 4. Capacitance

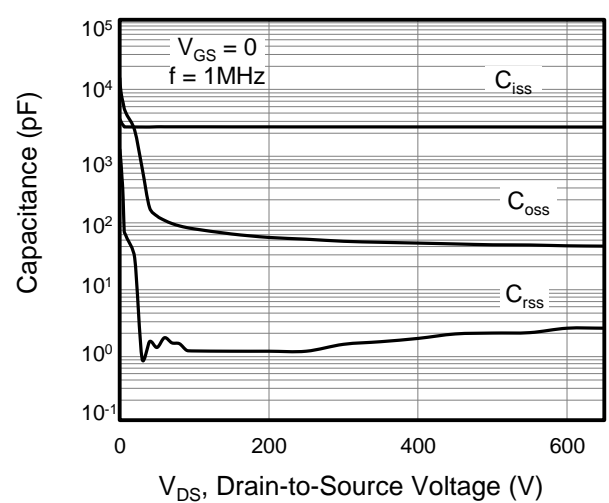


Figure 5. Gate Charge

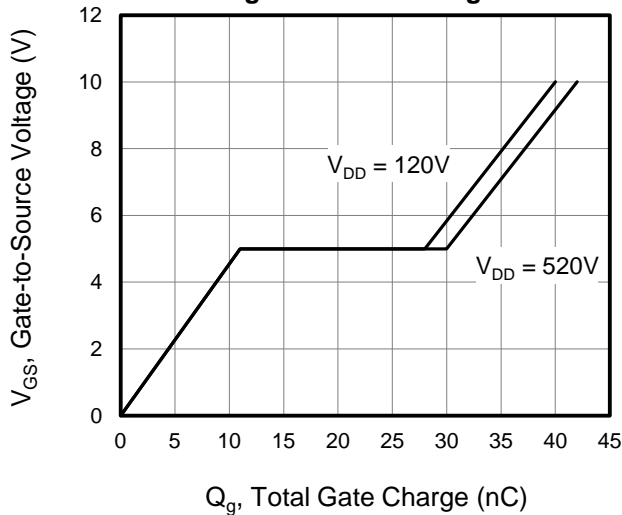
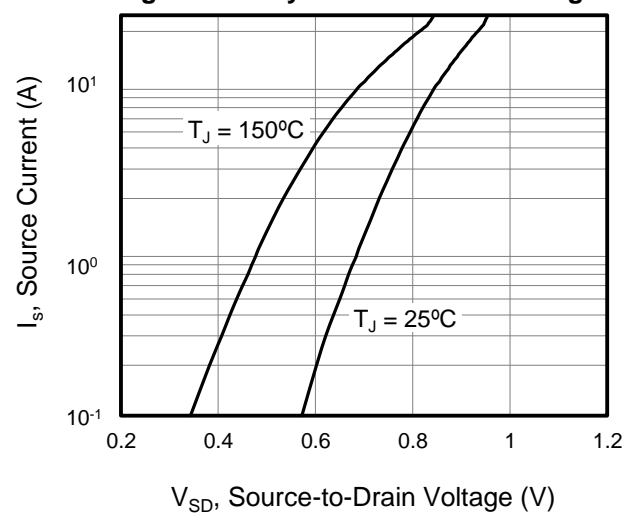


Figure 6. Body Diode Forward Voltage





Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. On-Resistance vs. Junction Temperature

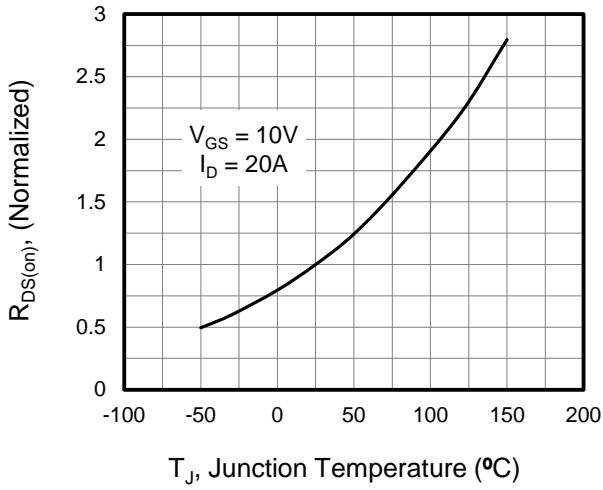


Figure 8. Breakdown voltage vs. Junction Temperature

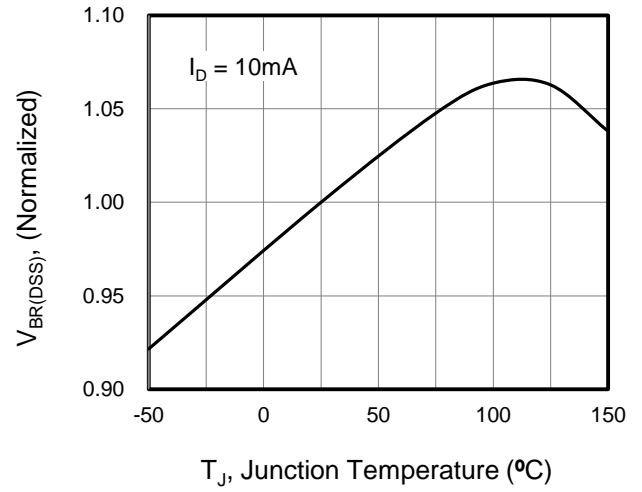


Figure 9. Transient Thermal Impedance

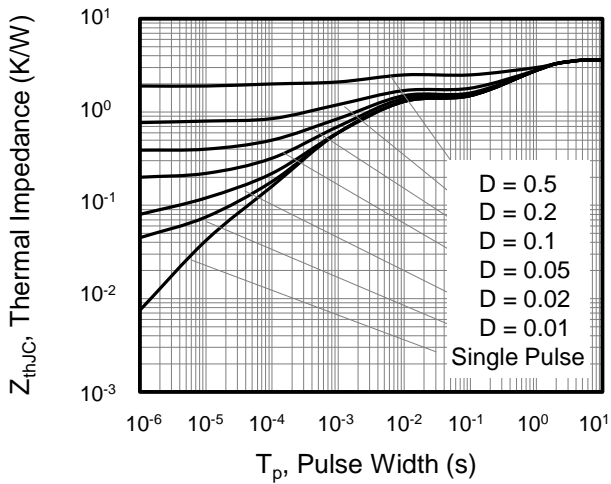


Figure 10. Safe operation area for

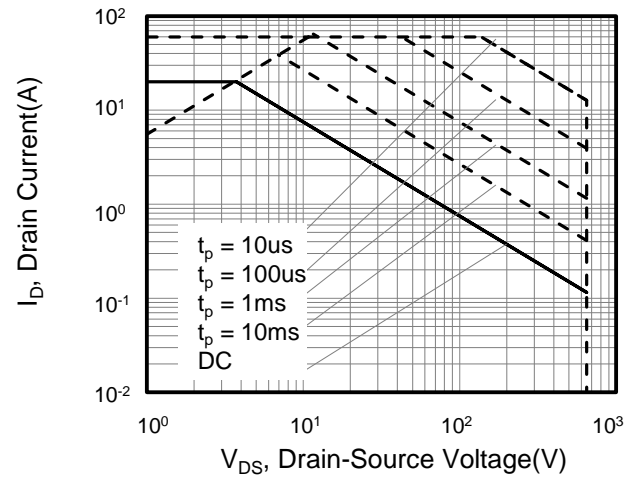




Figure A: Gate Charge Test Circuit and Waveform

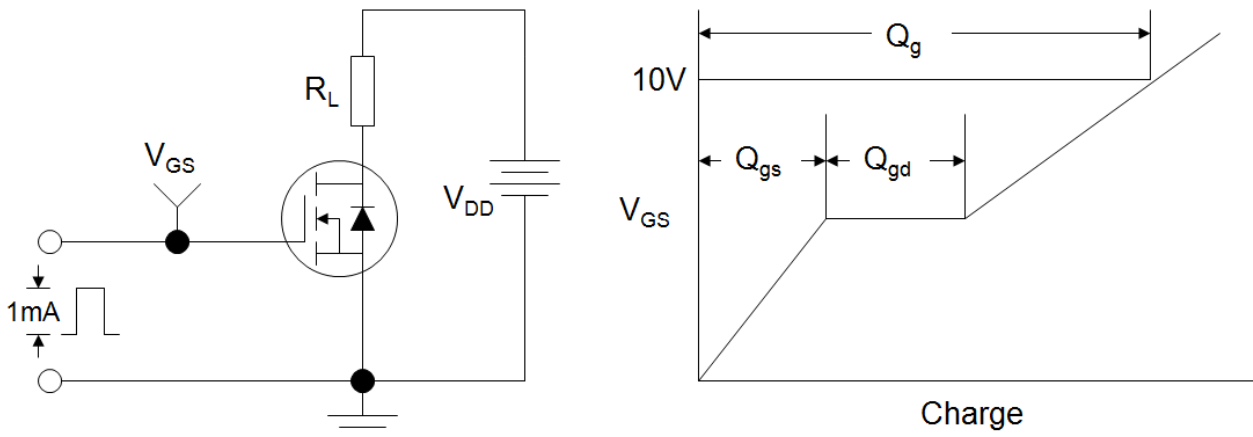


Figure B: Resistive Switching Test Circuit and Waveform

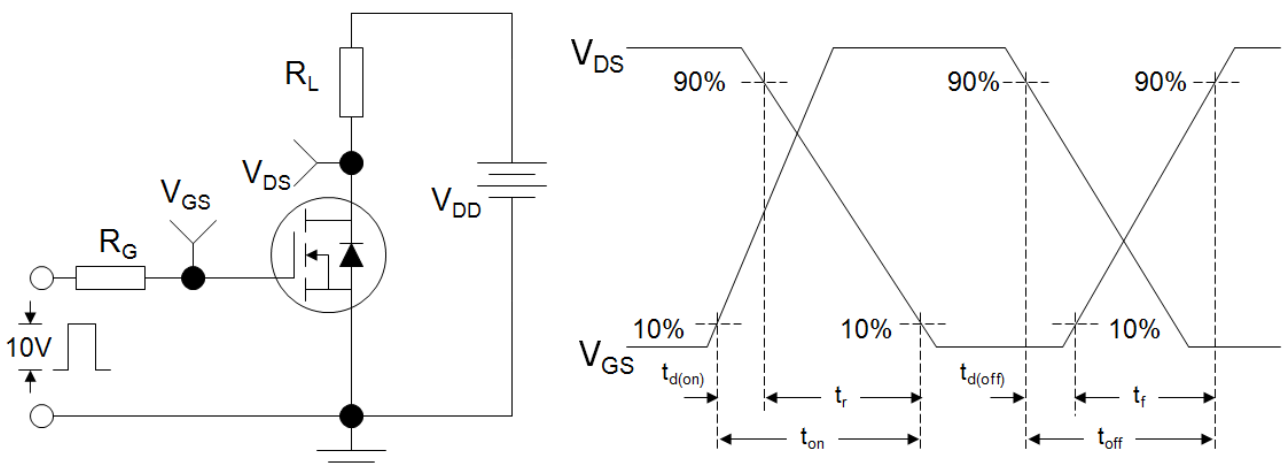
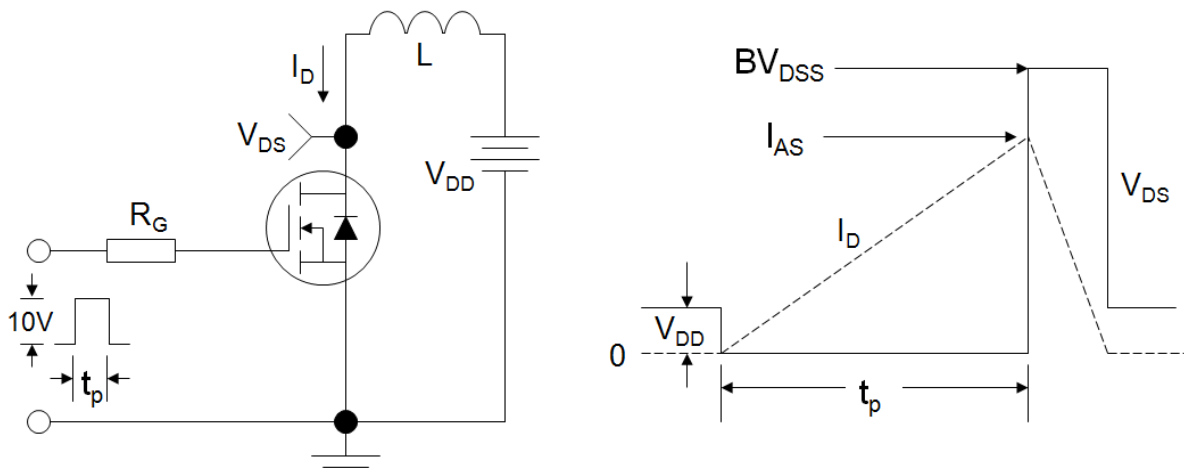
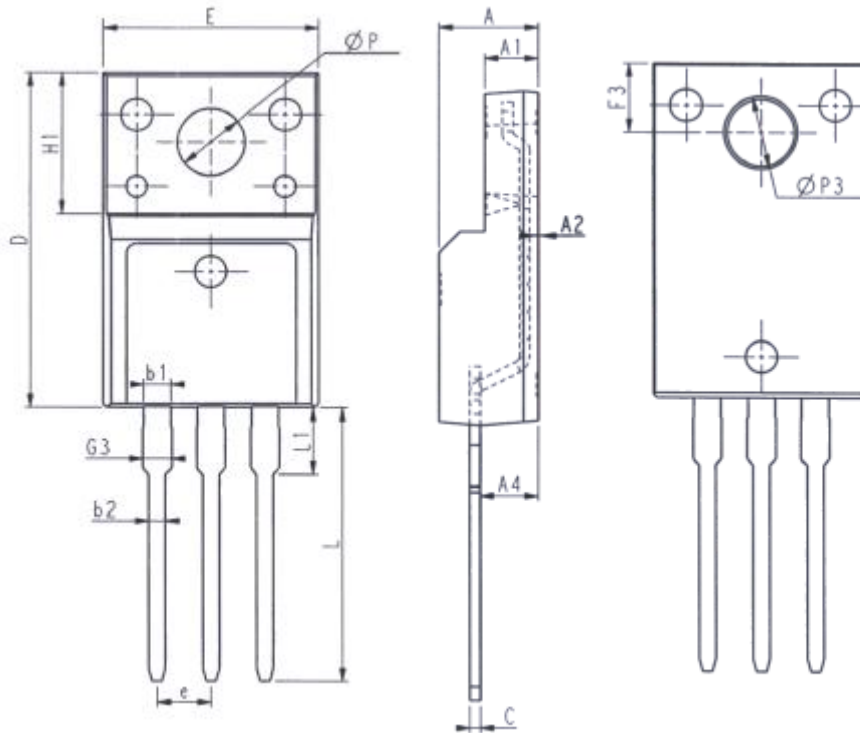


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



**TO-220F**

Unit: mm			Unit: mm		
Symbol	Min.	Max.	Symbol	Min.	Max.
E	9.96	10.36	L	12.68	13.28
A	4.50	4.90	L1	2.93	3.13
A1	2.34	2.74	P	3.03	3.38
A2	0.30	0.60	P3	3.15	3.65
A4	2.56	2.96	F3	3.15	3.45
c	0.40	0.65	G3	1.25	1.55
D	15.57	16.17	b1	1.18	1.43
H1	6.70REF		b2	0.70	0.95
e	2.54BSC				



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