



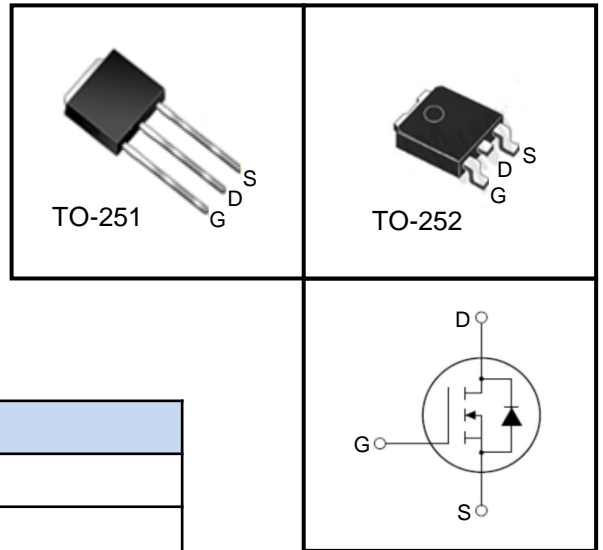
# 650V Super-Junction Power MOSFET

## FEATURES

- Very low FOM  $R_{DS(on)} \times Q_g$
- 100% avalanche tested
- RoHS compliant

## APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



Device Marking and Package Information		
Device	Package	Marking
TPU65R2K4A	TO-251	65R2K4A
TPD65R2K4A	TO-252	65R2K4A

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , unless otherwise noted				
Parameter	Symbol	Value		Unit
		TO-251	TO-252	
Drain-Source Voltage ( $V_{GS} = 0\text{V}$ )	$V_{DSS}$	650		V
Continuous Drain Current	$I_D$	2.1		A
Pulsed Drain Current (note1)	$I_{DM}$	6.3		A
Gate-Source Voltage	$V_{GSS}$	$\pm 30$		V
Single Pulse Avalanche Energy (note2)	$E_{AS}$	5		mJ
Avalanche Current (note1)	$I_{AR}$	2.1		A
Repetitive Avalanche Energy (note1)	$E_{AR}$	0.05		mJ
Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	30		W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55~+150		$^\circ\text{C}$

Thermal Resistance				
Parameter	Symbol	Value		Unit
		TO-251	TO-252	
Thermal Resistance, Junction-to-Case	$R_{thJC}$	4.1		K/W
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	75		



Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	$\mu A$
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	--	--	100	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5	--	3.5	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 1A$	--	2.16	2.42	$\Omega$
Forward Transconductance (Note3)	$g_{fs}$	$V_{DS} = 10V, I_D = 2A$	--	2	--	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = 50V,$ $f = 1.0\text{MHz}$	--	300	--	$\mu F$
Output Capacitance	$C_{oss}$		--	115	--	
Reverse Transfer Capacitance	$C_{rss}$		--	3.5	--	
Total Gate Charge	$Q_g$	$V_{DD} = 480V, I_D = 2A,$ $V_{GS} = 10V$	--	6.5	--	nC
Gate-Source Charge	$Q_{gs}$		--	1	--	
Gate-Drain Charge	$Q_{gd}$		--	3	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 300V, I_D = 2A,$ $R_G = 25\Omega$	--	9	23	ns
Turn-on Rise Time	$t_r$		--	25	55	
Turn-off Delay Time	$t_{d(off)}$		--	19	46	
Turn-off Fall Time	$t_f$		--	16	38	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	2.1	A
Pulsed Diode Forward Current	$I_{SM}$		--	--	6.3	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = 2A, V_{GS} = 0V$	--	0.95	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R = 480V, I_F = I_S,$ $di_F/dt = 100A/\mu s$	--	210	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	1	--	$\mu C$
Peak Reverse Recovery Current	$I_{rrm}$		--	8	--	A

**Notes**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 1A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width  $\leq 300\mu s, \text{Duty Cycle } \leq 1\%$



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )

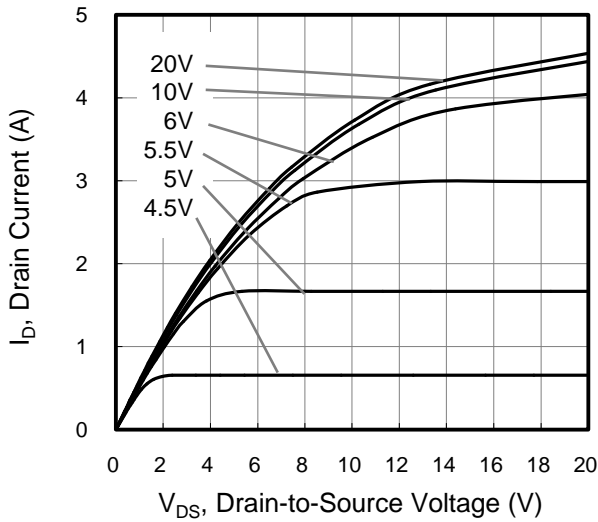


Figure 2. Output Characteristics ( $T_J = 150^\circ\text{C}$ )

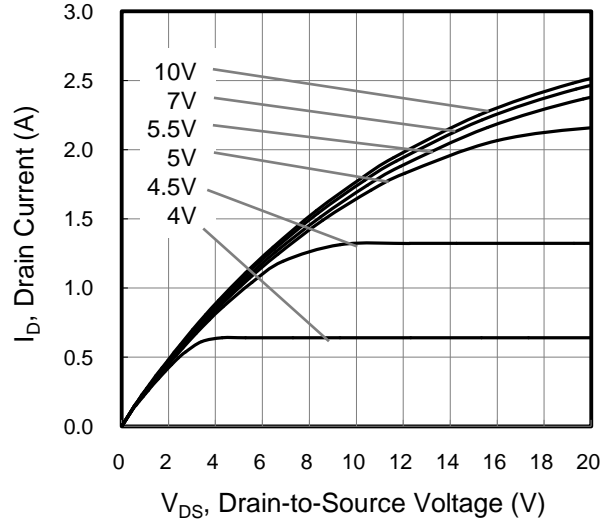


Figure 3. On-Resistance vs. Drain Current

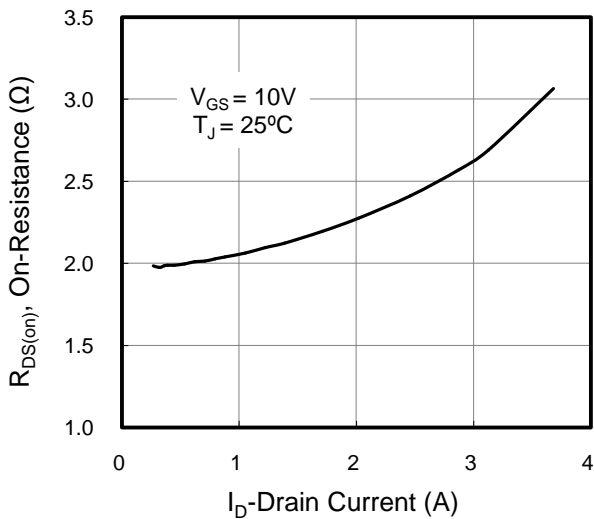


Figure 4. On-Resistance vs. Temperature

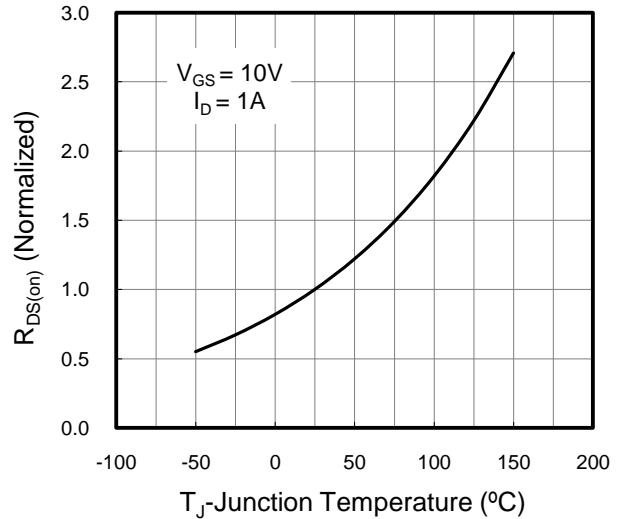


Figure 5. Transfer Characteristics

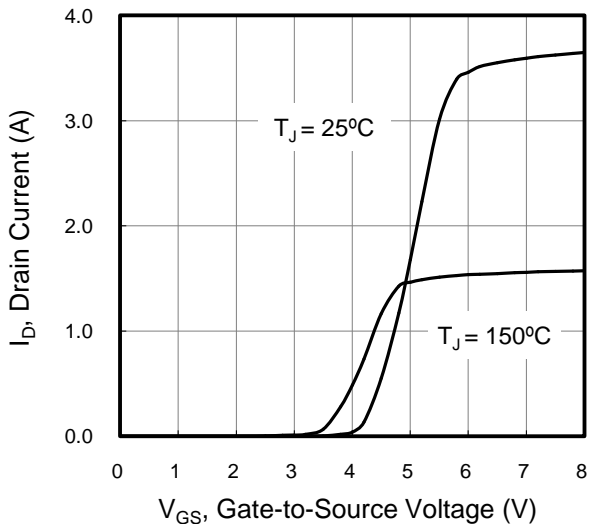
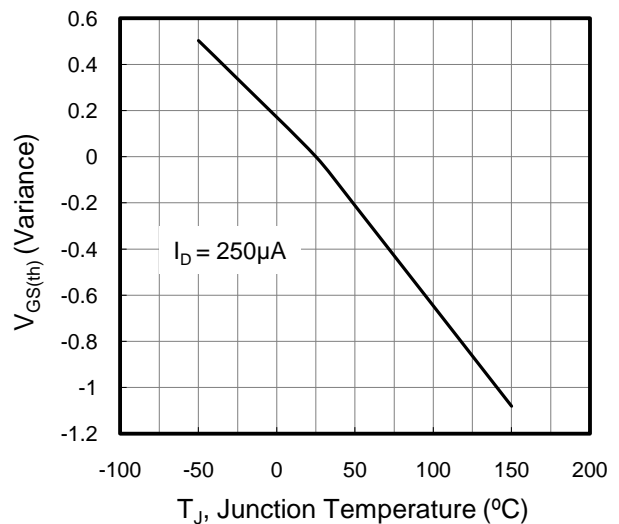


Figure 6. Threshold Voltage vs. Temperature





Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Capacitance

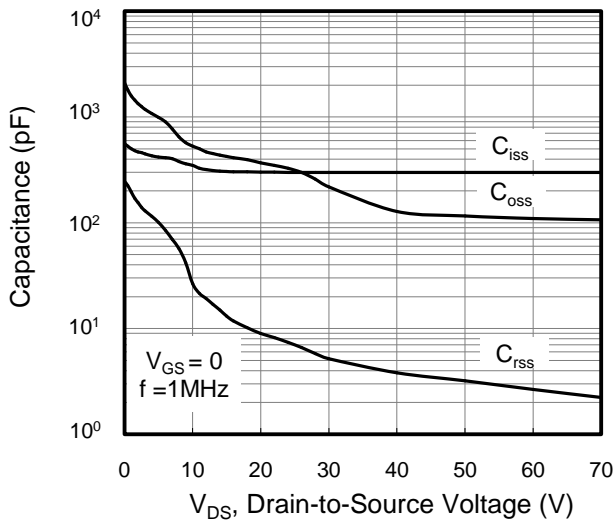


Figure 8. Gate Charge

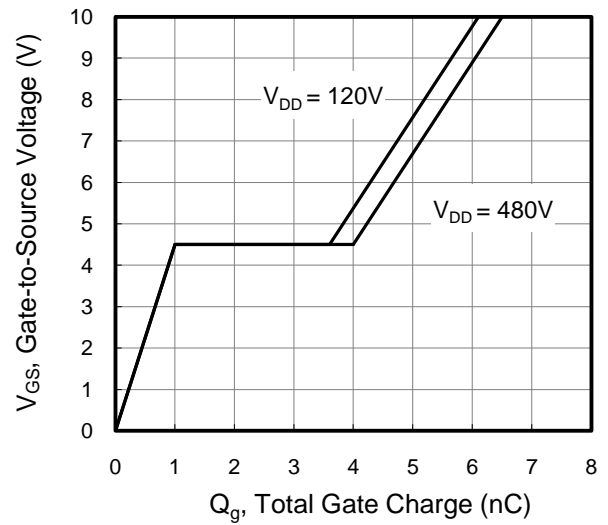


Figure 9. Body Diode Forward Voltage

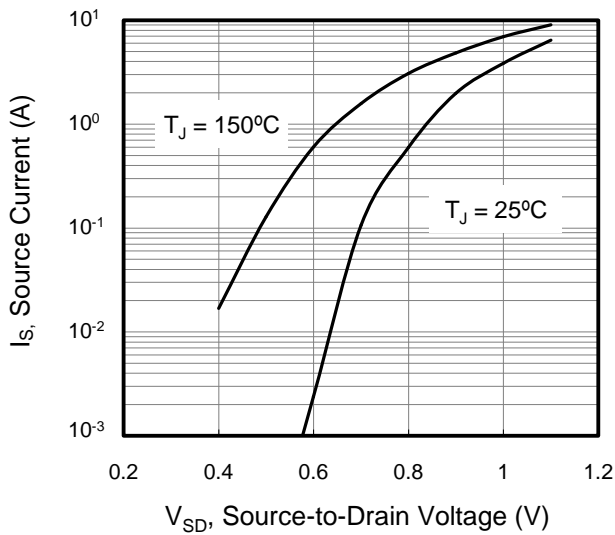


Figure 10. Transient Thermal Impedance

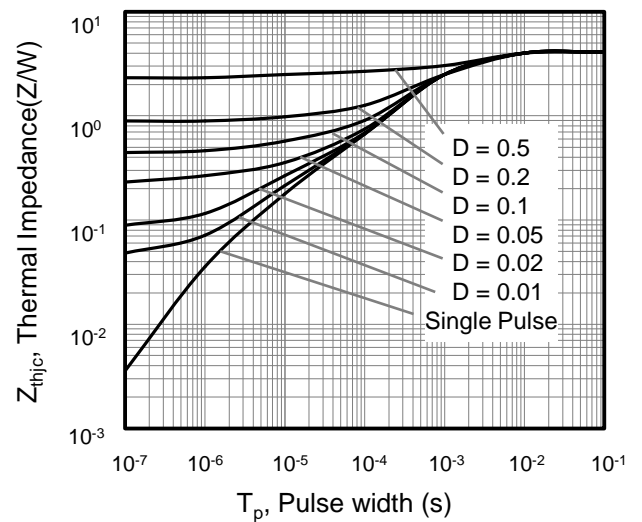




Figure A: Gate Charge Test Circuit and Waveform



Figure B: Resistive Switching Test Circuit and Waveform

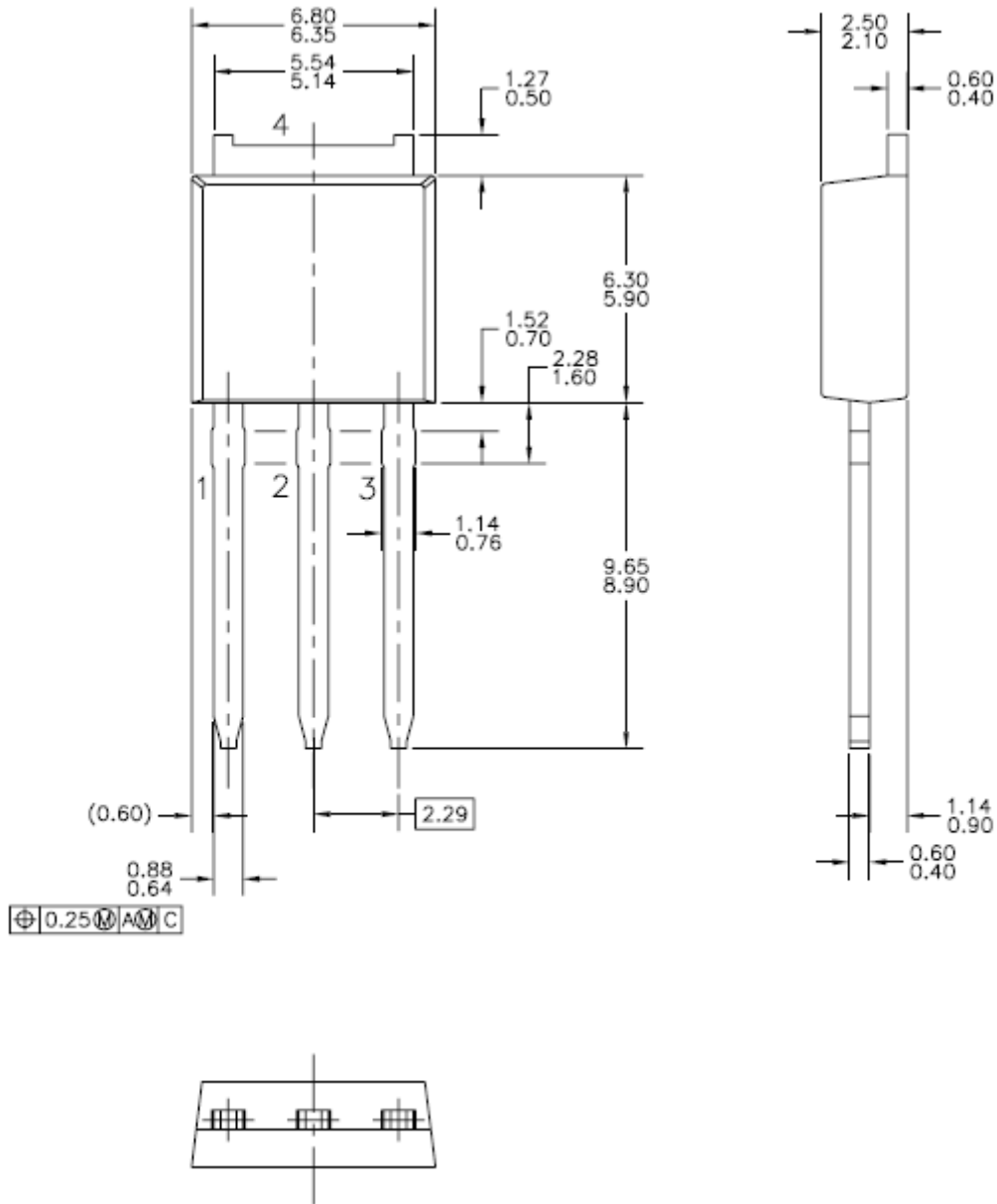


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



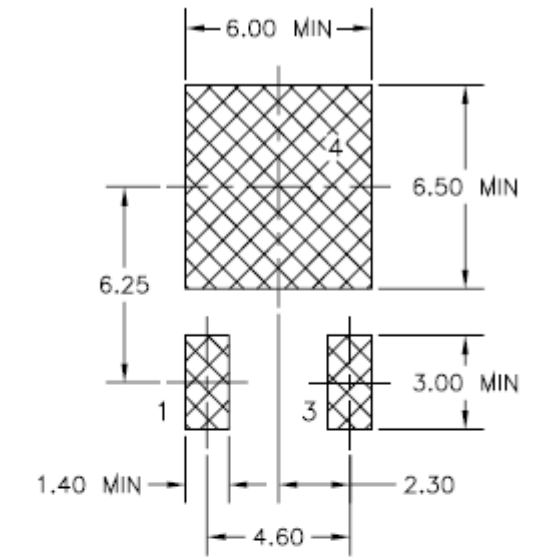
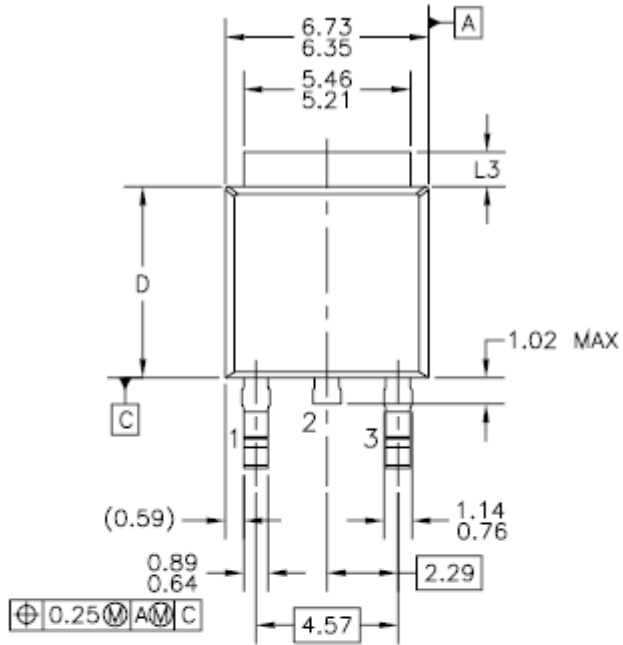


# TO-251

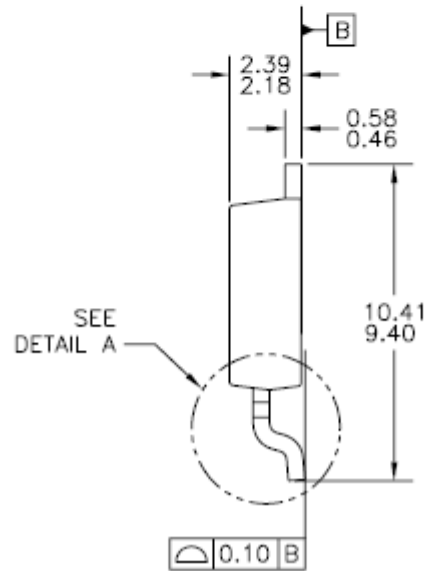
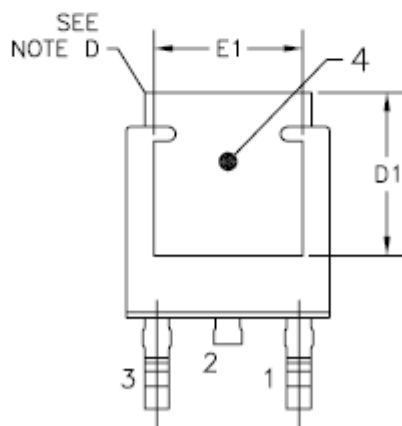




# TO-252



LAND PATTERN RECOMMENDATION





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